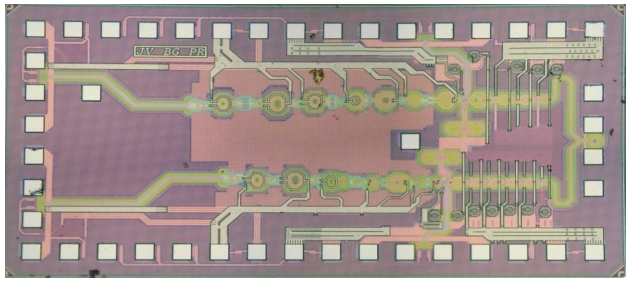
ESD in RF and mmWave ICs

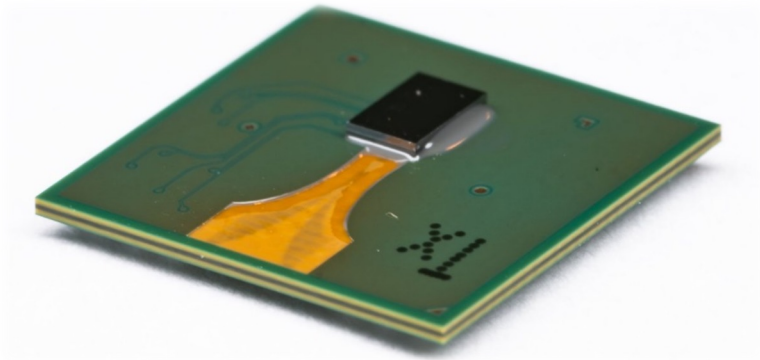
Presentation at Incize 10 years Anniversary

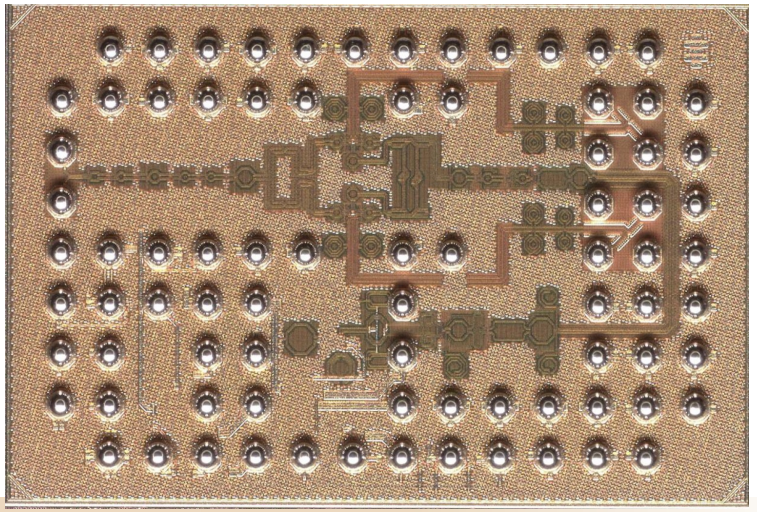
By Joren Vaes – April 26TH 2024

Introduction

- M.Sc. 2018, PhD 2024 @ KU Leuven
- PhD Topic: Polymer Microwave Fiber as a High Data Rate Channel
  - Achieved 100 Gbit/second over 3 meters at D-band
  - Package, antenna and chip design up to 170 GHz
  - High-speed IO up to 56 Gb/s PAM4
- Now at Sofics, working on high-speed IO portfolio







Sofics: Provider of I/O chip interface IP

Robust circuit solutions

Custom I/O cells, Over-voltage tolerant IOs, LIN/CAN PHY

PhyStar

On-chip ESD protection for low voltage/advanced processes

Analog I/Os and on-chip ESD protection down to 2 nm

TakeCharge

On-chip ESD protection for high voltage and BCD processes

Clamps for 5 V up to 50 V, Automotive, Industrial

PowerQubic

Sofics

- Experience with high-speed IO and RF
  - >1kV HBM ESD clamp for 112 Gbps SERDES (5 nm TSMC)
  - Up to 50% lower equivalent cap than foundry-supplied dual-diode solutions
  - RF limiting/clipping circuits for NFC
  - ESD for 8.5 GHz LNA
  - 40% of Bluetooth transceivers sold today

Nearly 100 customers and 10 foundry partners

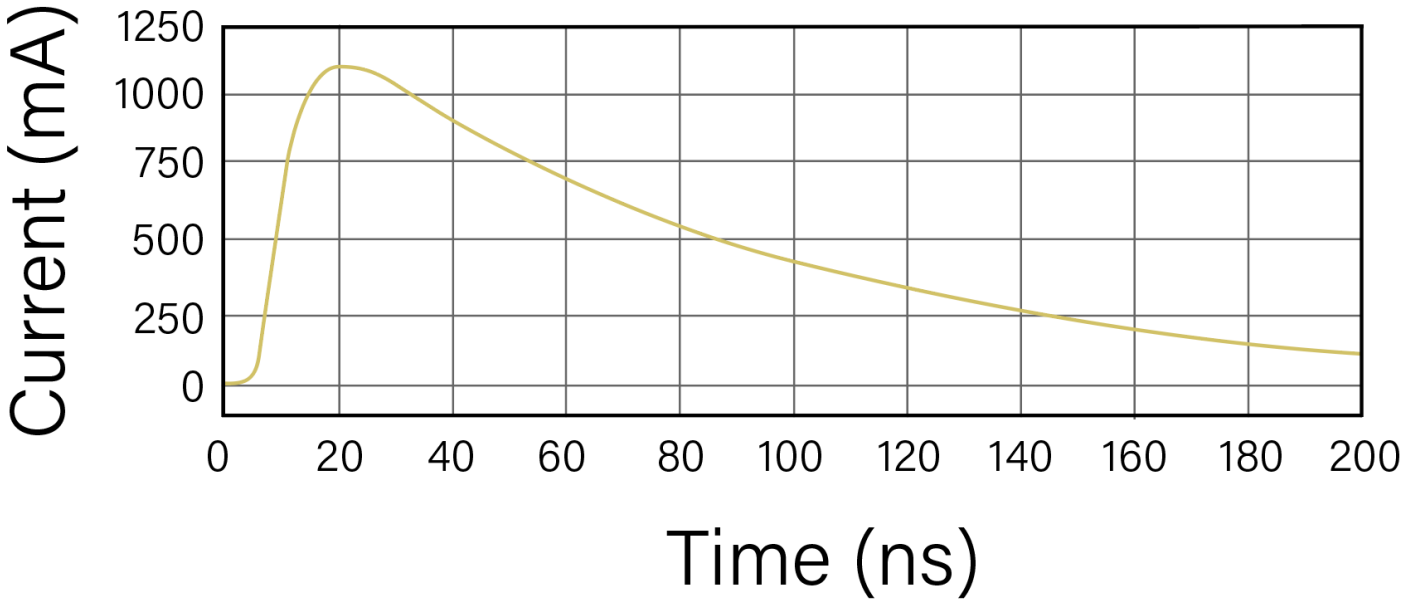
Overview of my talk

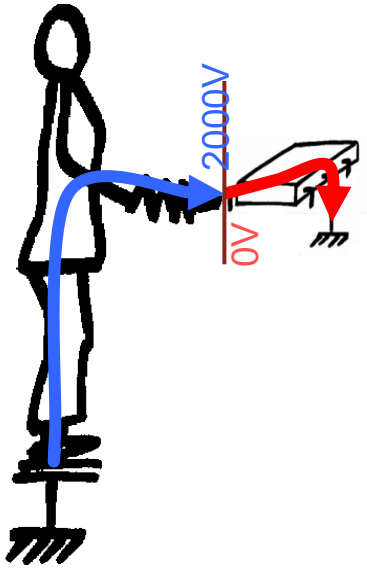
- About Sofics and me
- Introduction to ESD: HBM? CDM?
- ESD problems in high-speed and RF circuits
- 4 ways to integrated to protect against ESD in high-speed and RF circuits
- Conclusion

Refresher on ESD

ESD: HBM

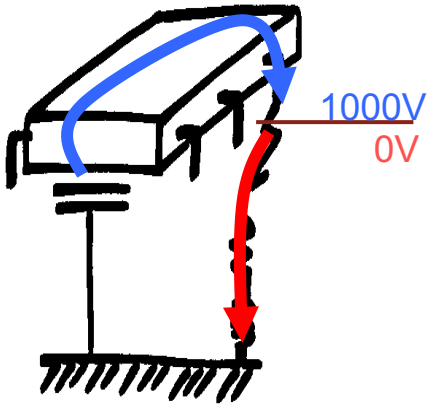
- HBM: Human-body model
  - 100 pF charged to a certain voltage, then discharged into DUT through 1.5k resistor
  - Between any two pins of your DUT
  - Risetime on the order of 10-20 ns

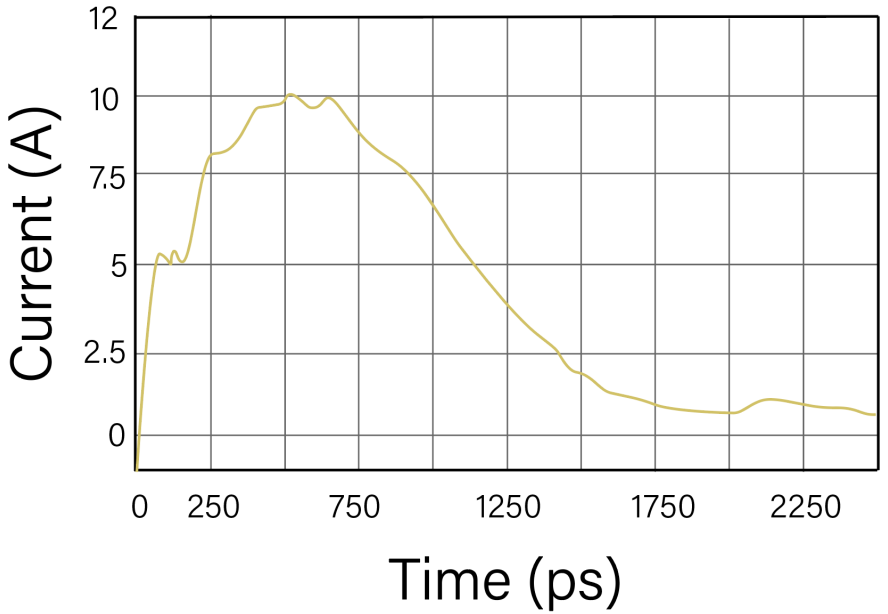




ESD: CDM

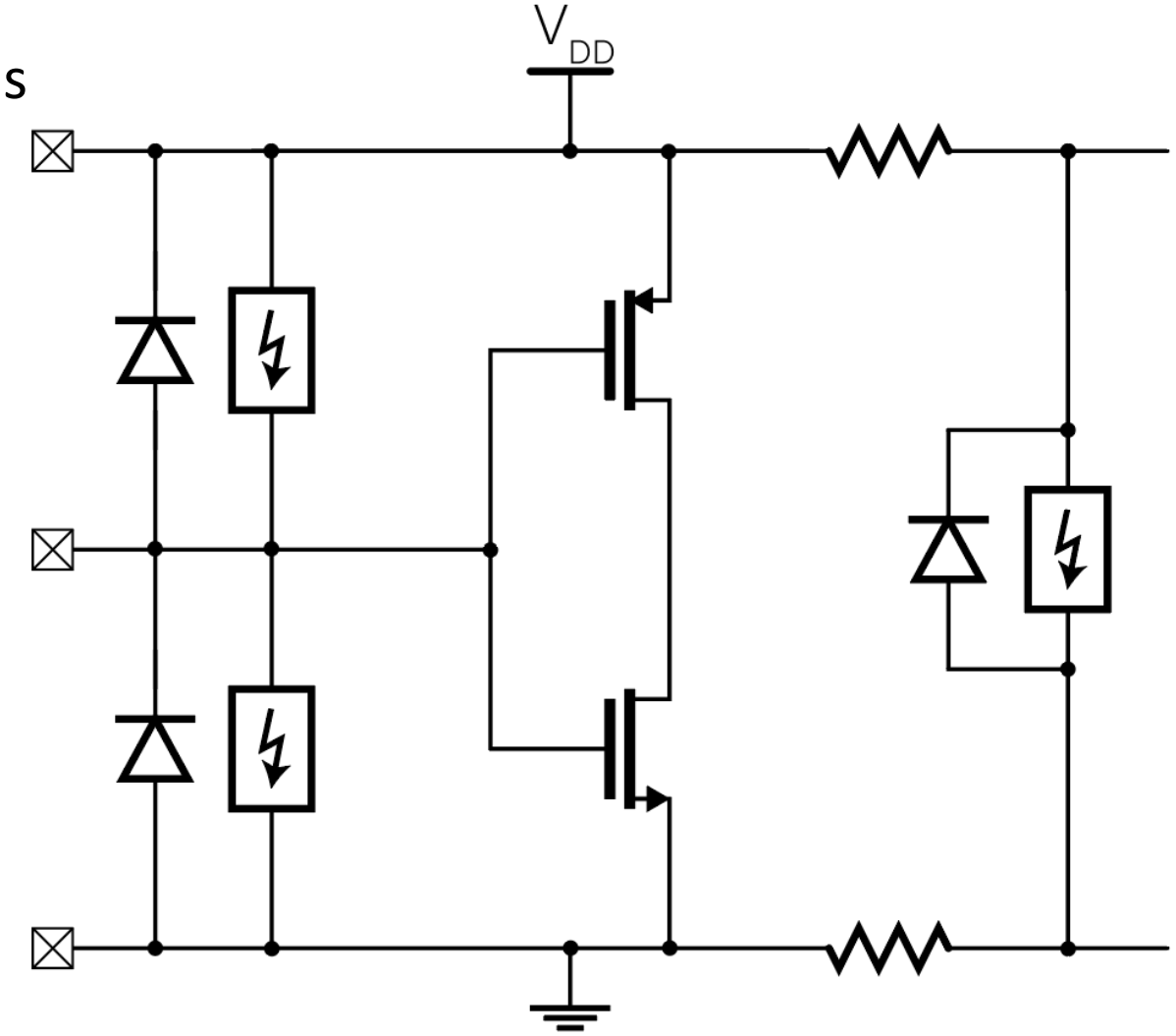
- CDM: Charged device model
  - DUT itself is charged up w.r.t. ‘ground’, then discharged through a single bondpad/pin
  - All structures are under stress (as all internal nodes are assumed charged)
  - Harder to quantify exact requirements for IO, as chip area defines capacitance, and each pad can have a different inductance
- Pulse can have risetime <100 ps for modern packages
  - Spectral content > 1 GHz!





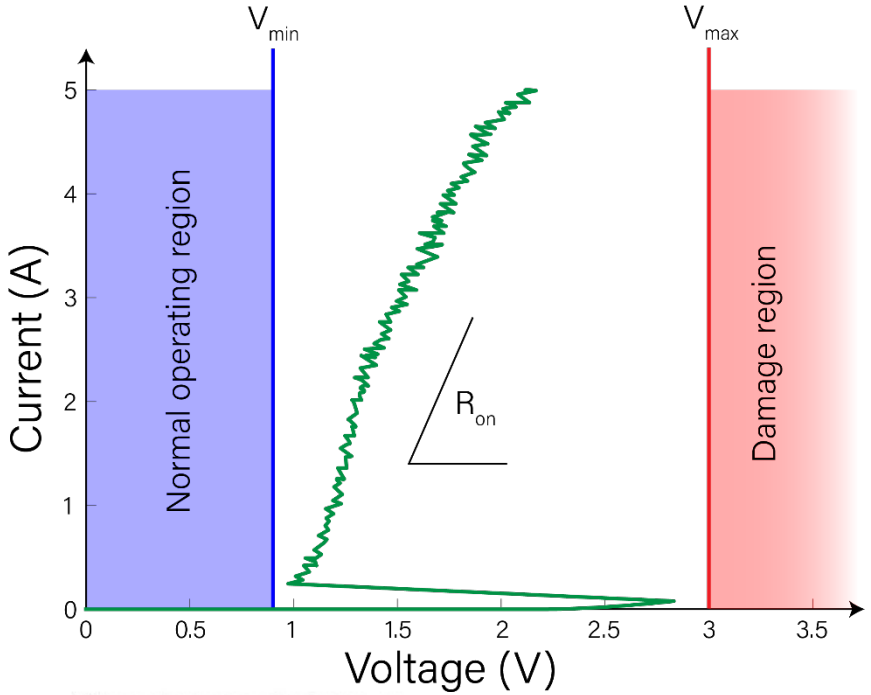
How do we protect circuits?

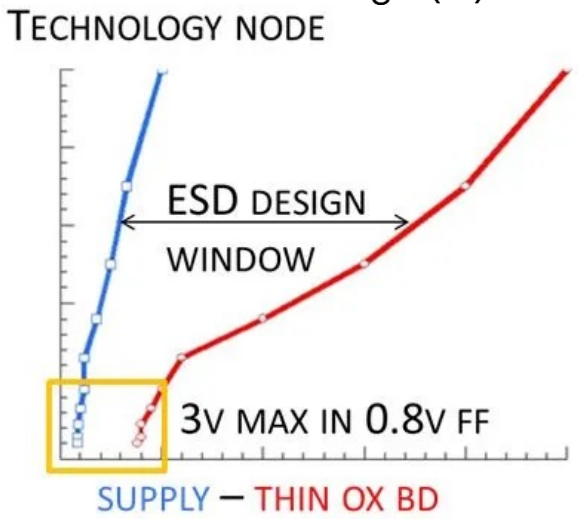
- Place ESD devices between IO's and supplies
- Add supply clamps between supplies
- Provide path for ESD current to flow



ESD window

- ESD protection must be invisible at normal voltages (Vmin)
- Maximum voltage must never exceed maximum threshold
- ESD device must handle sufficient current
- Difference between Vmin and Vmax is decreasing with newer technologies

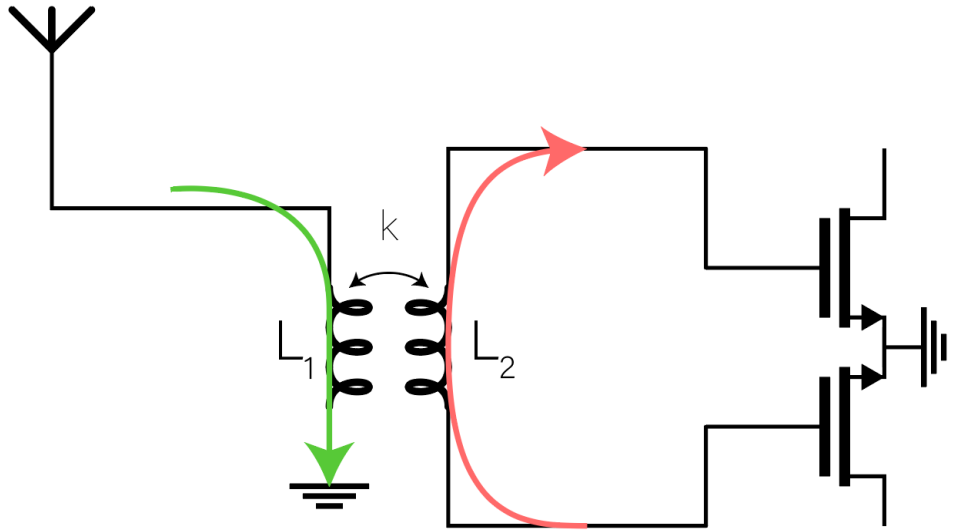




Specifics for RF structures

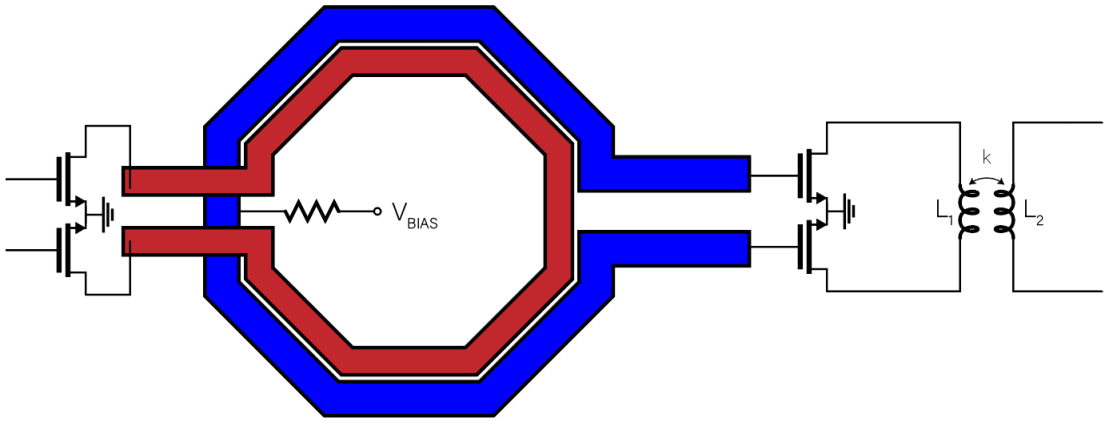
But for RF Circuits: Don’t transformers block ESD?

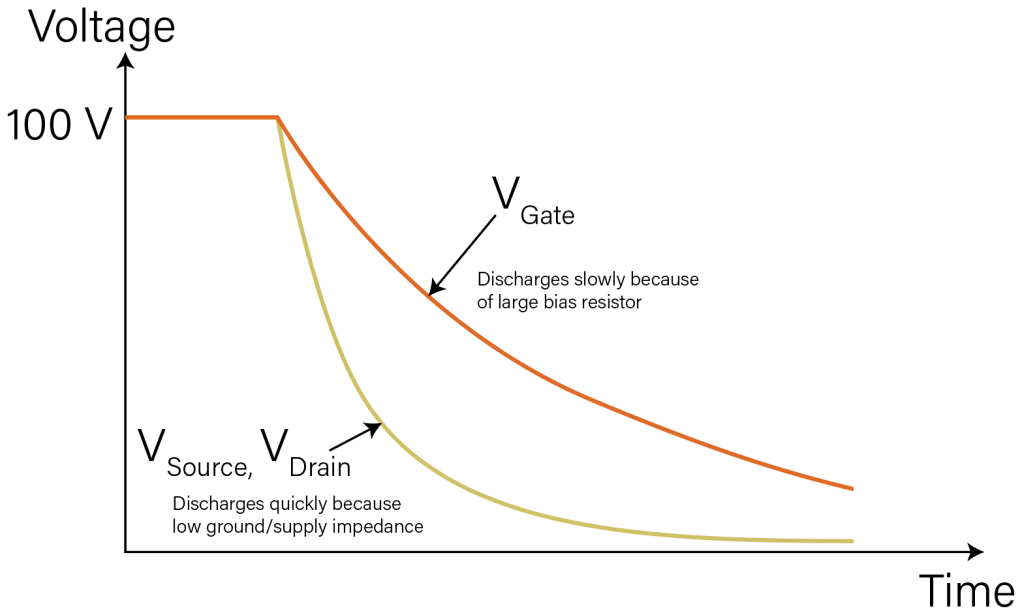
- HBM: Sure!
- CDM pulse high frequency (strong content > 1 GHz)
- Even with strong attenuation, induced currents can still cause large voltages to appear across devices
- Proper simulation and modeling needed
- Where do you put the ESD protection device? Primary? Secondary? Both?
- Is it sufficient to put it at centertap?
  - CDM Current induces differential voltage, so not really!



But ESD is just a I/O problem, right?

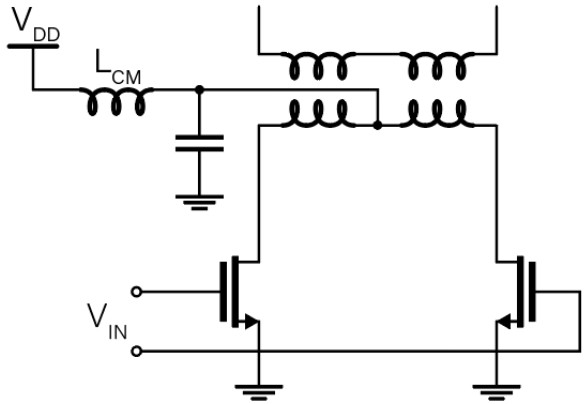
- CDM!
  - Secondary often only connected to gates of next stage and big resistor
  - Gate discharges slowly, but source connected to ground, which discharges rapidly
  - Need to take this into account!
  - ESD protection at core of your RF path might be needed

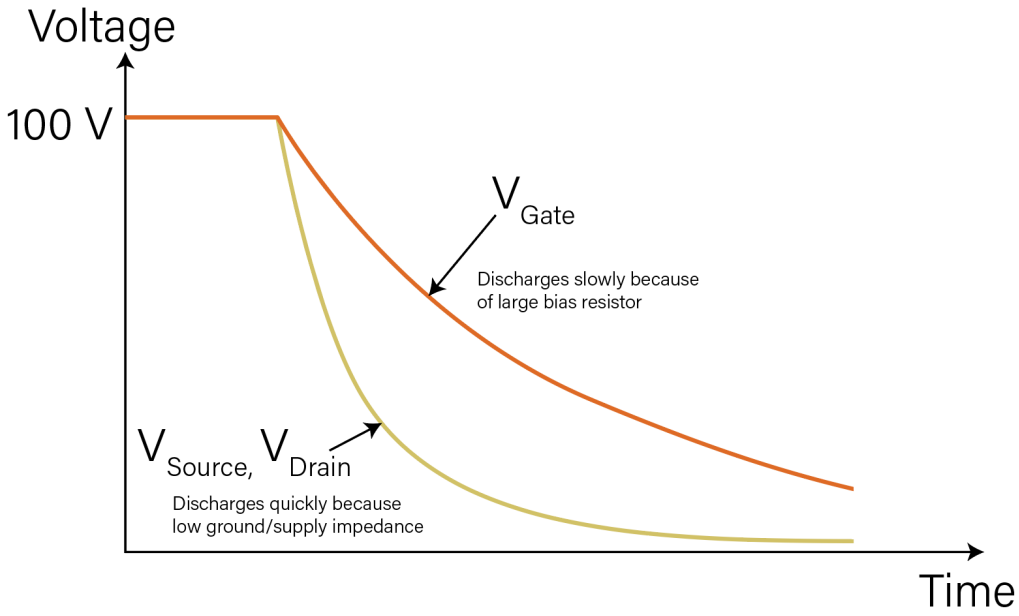




But ESD is just a I/O problem, right?

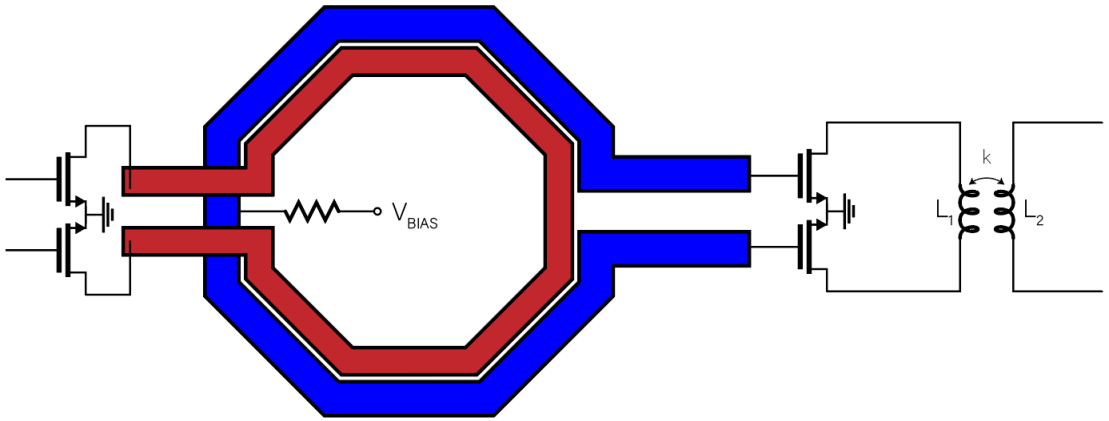
- CDM!
  - Similar story for supply when a common-mode choke is used
  - Might have large local decap behind choke to create low-impedance supply
  - But impedance to pad will be higher, which will result in large voltages during CDM events

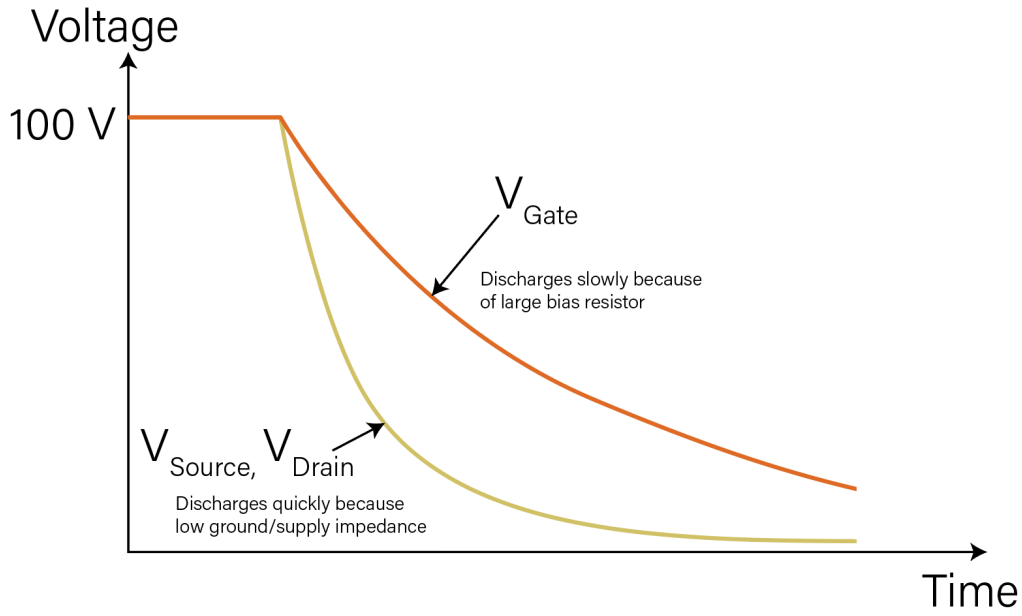




How to solve these issues?

- ESD expertise is required
- Add small local clams to each node with significant capacitance but without a low-impedance path to the supply pads





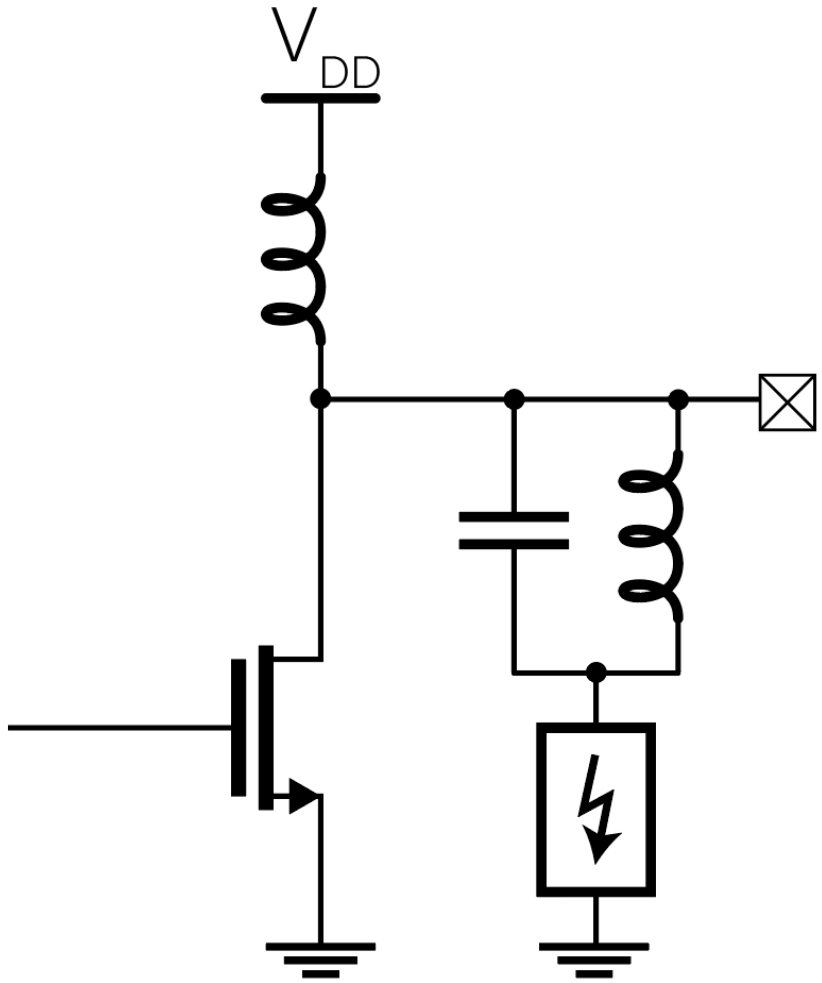
High speed ESD

How do we make ESD invisible for High-speed applications?

- Method 1: Reduce capacitance of ESD
  - Use expertise to design and tune local ESD clamps to application
  - But still treat the ESD as a parasitic
  - Sofics has provided such low-cap ESD solutions for applications up to 8.5 GHz

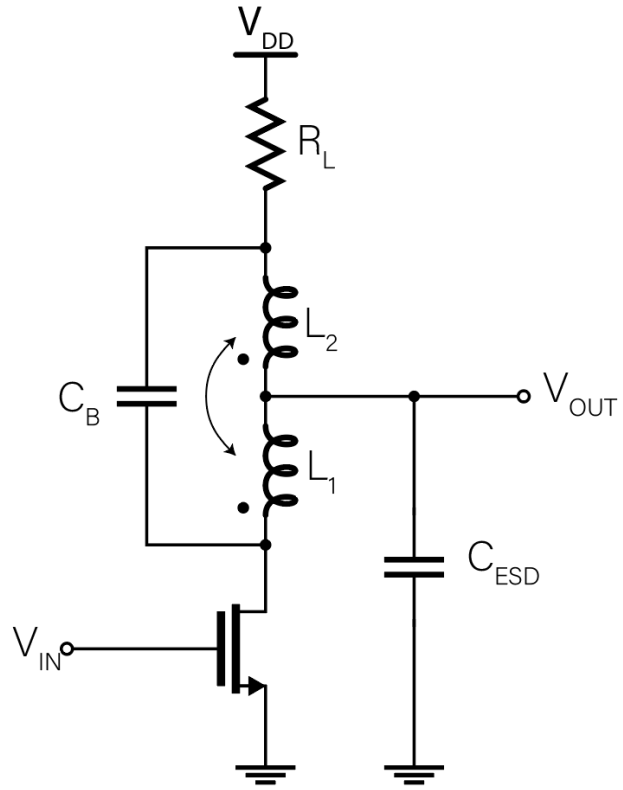
How do we make ESD invisible for High-speed applications?

- Method 2: Use LC trap to hide ESD devices
  - Tune LC trap to act as open for operation frequency
  - Only works for narrowband circuits
  - Only works at sufficiently high frequencies
    - At lower frequencies, inductor would also block (part) of the current, and result in too high voltages



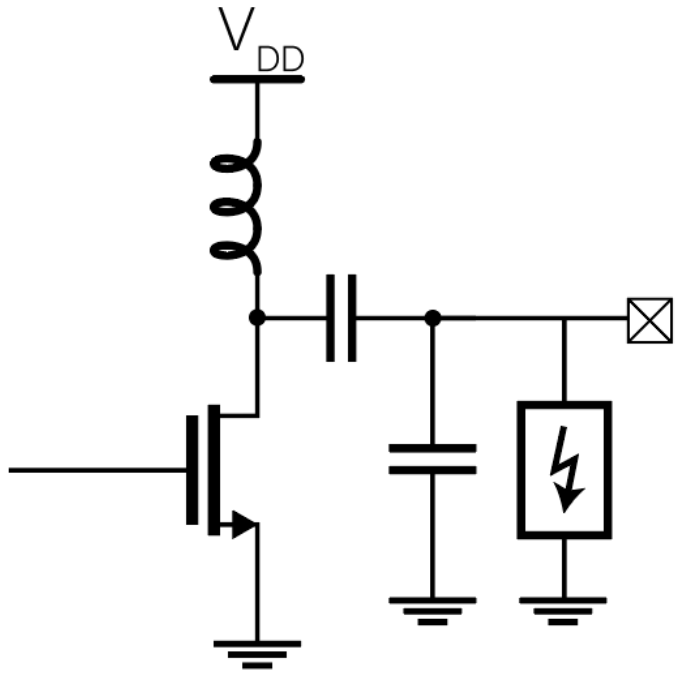
How do we make ESD invisible for High-speed applications?

- Method 3: Co-design with Tcoils and similar tuning
  - Broadband networks
  - Requires accurate knowledge of the ESD capacitance to work optimally
    - And ESD capacitance must be stable over wide frequency
  - Communication with ESD provider is crucial



How do we make ESD invisible for High-speed applications?

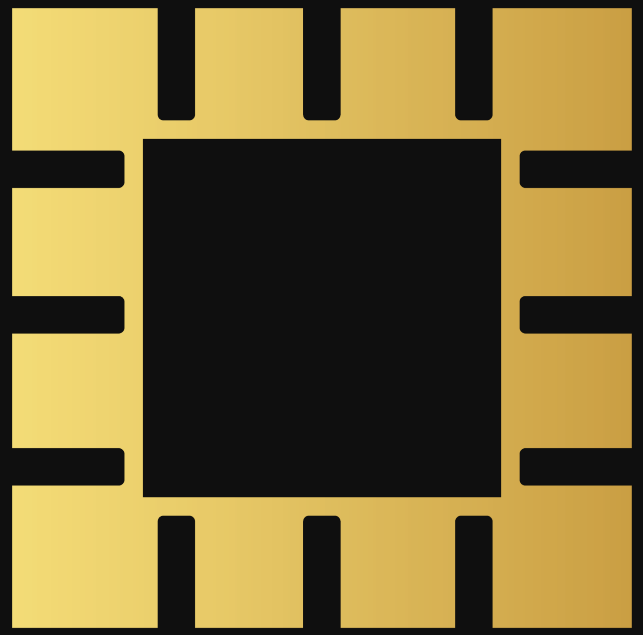
- Method 4: make the ESD a part of the matching/RF network
  - (partially) Replace a shunt capacitor to RF ground with an ESD cell
  - The capacitance and Q-factor of the ESD cell now becomes very important
  - Accurate modeling essential



Conclusion

Conclusion

- For high speed and RF, we cannot separate the ESD design from the IO design
- CDM stress forces us to consider protection also deep inside the signal path
- By considering the ESD requirements early in the design process we can ensure high performance
- Low-cap ESD solutions combined with circuit techniques to ‘hide’ them allows for state-of-the-art performance



Sofics

Solutions for ICs