Advanced porous silicon substrate for RF applications

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IQE

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Agenda

- Introduction to Porous Silicon
- Porous Silicon Resistivity
- RF Characterisation of Porous Silicon
- Epitaxy on Porous Silicon
- Conclusions

Introduction to porous silicon

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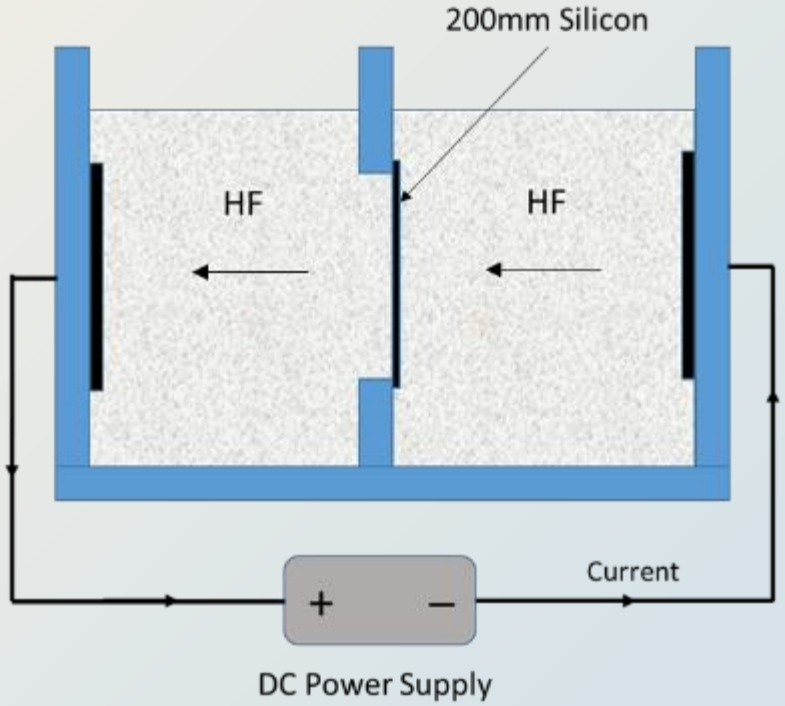
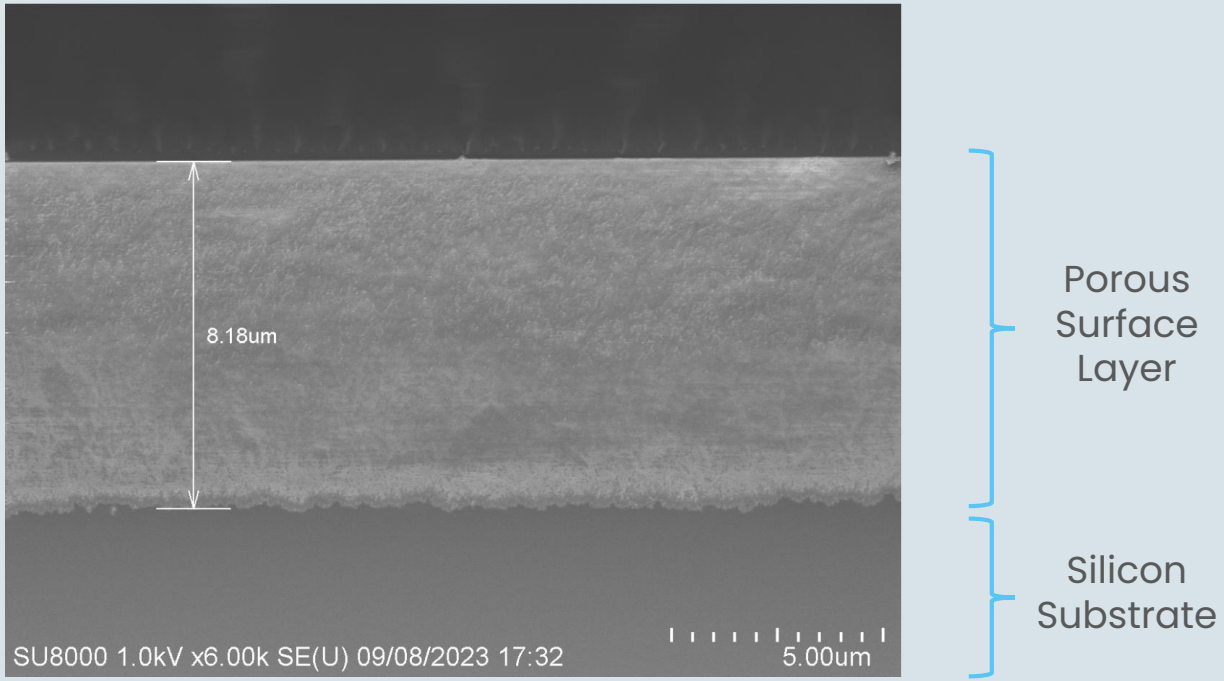
What is porous silicon?

Porous Silicon:

Electrochemical Etch of Silicon in Hydrofluoric Acid.

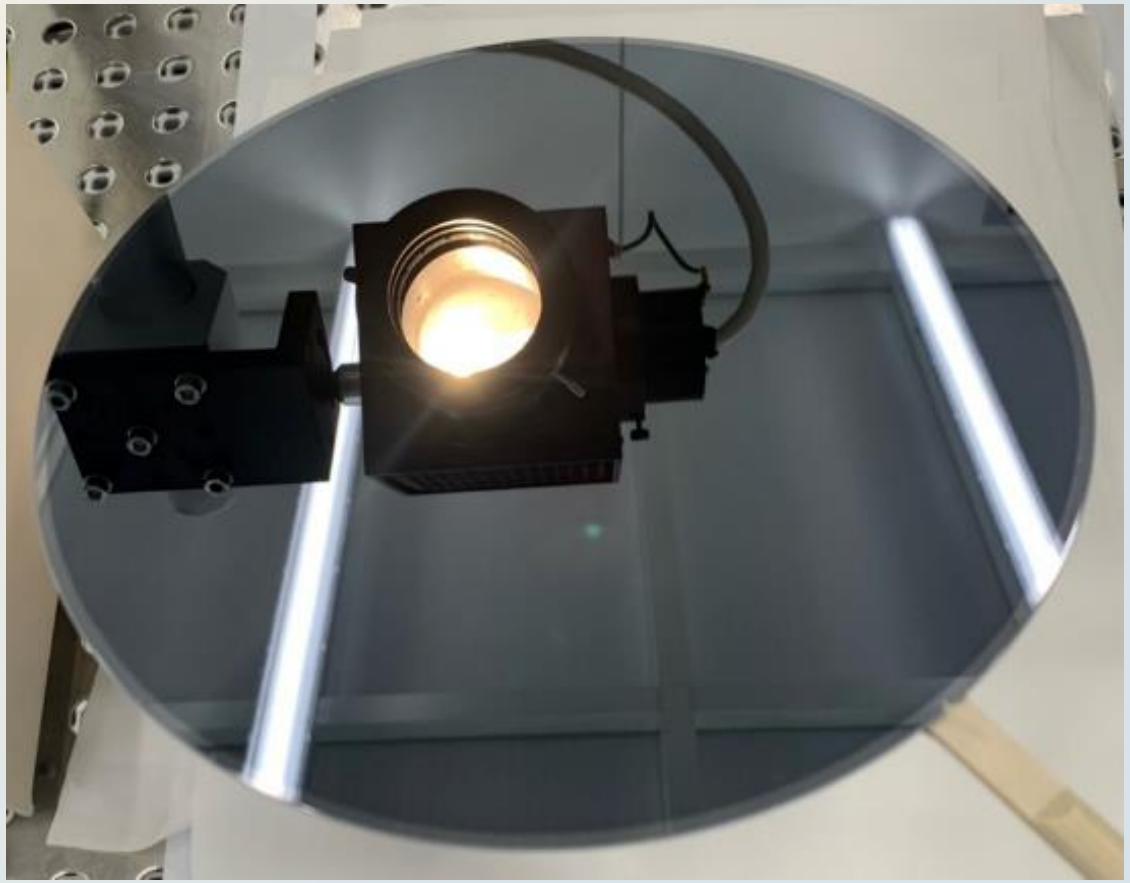


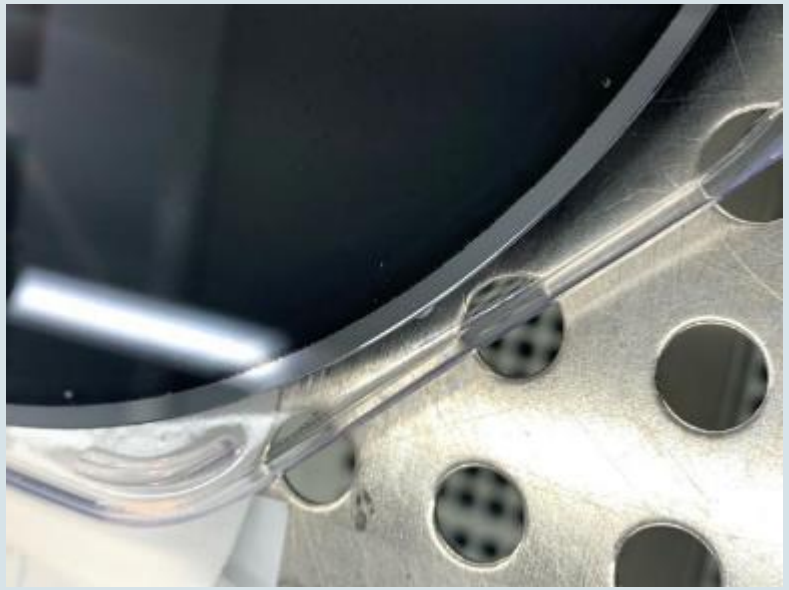
XSEM:



Etch duration ~ 5mins

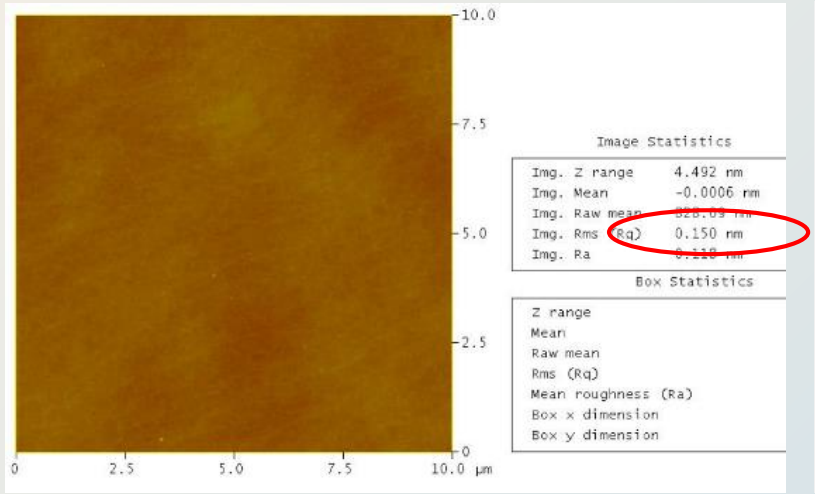
200mm porous silicon

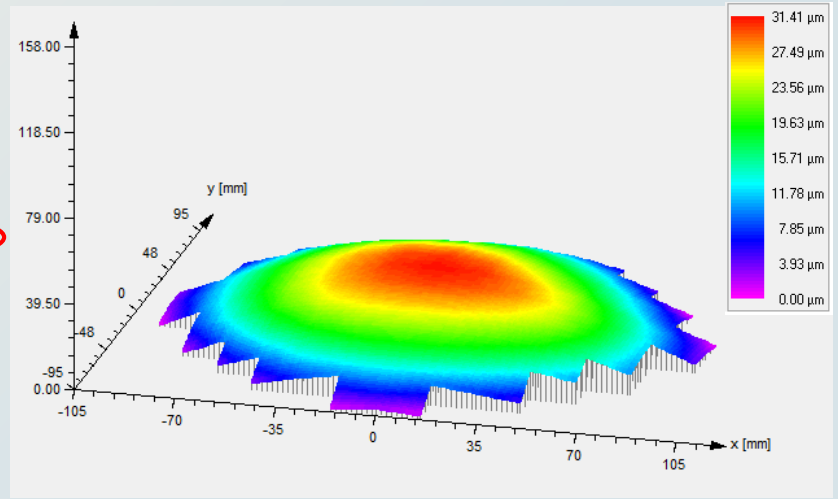




- Typical bright light image of a 200mm porous silicon substrate
- Industry standard 3mm edge exclusion

Porous silicon





Roughness & bow

Si(100)

Average:	15.86 µm	[6.7um]
Standard deviation:	8.75 µm	
Peak-to-Valley:	31.41 µm	[16.7um]
PV horizontal:	28.35 µm	
PV vertical:	29.02 µm	
Radius horizontal:	-162.12 m	
Radius vertical:	-169.31 m	

Post Thermal Anneal

AFM:

- Ultra smooth surface post porous etch
- On a par with prime silicon surface roughness

Porous silicon resistivity

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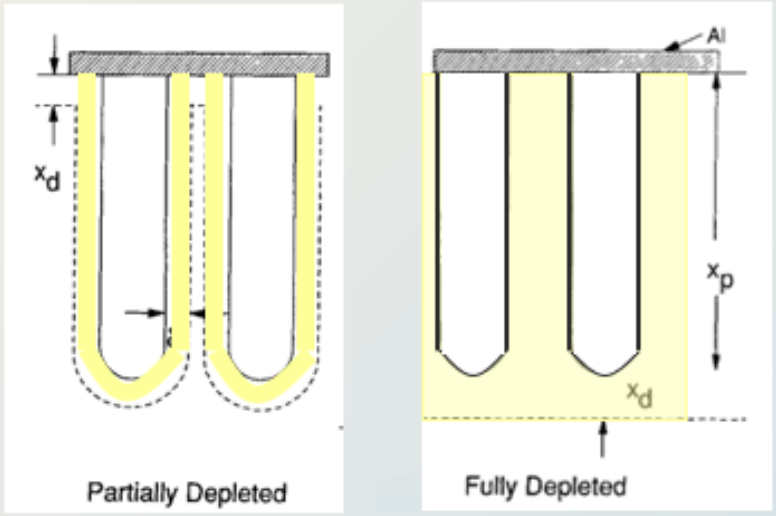
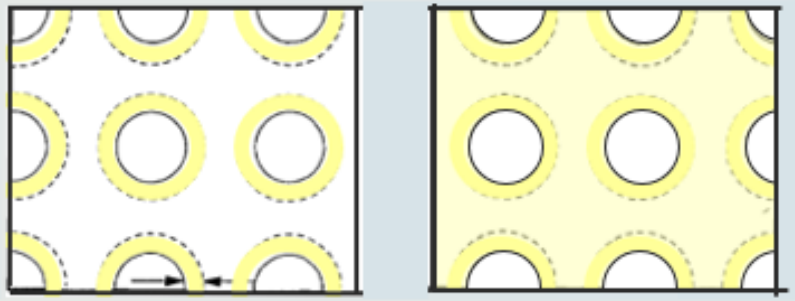
Porous silicon resistivity

Cross Section



Plan View



Investigations of the Electrical Properties of Porous Silicon

Rolfe C. Anderson, Richard S. Muller, and Charles W. Tobias*

Berkeley Sensor and Actuator Center, Department of Electrical Engineering and Computer Science, University of California, Berkeley, California 94720

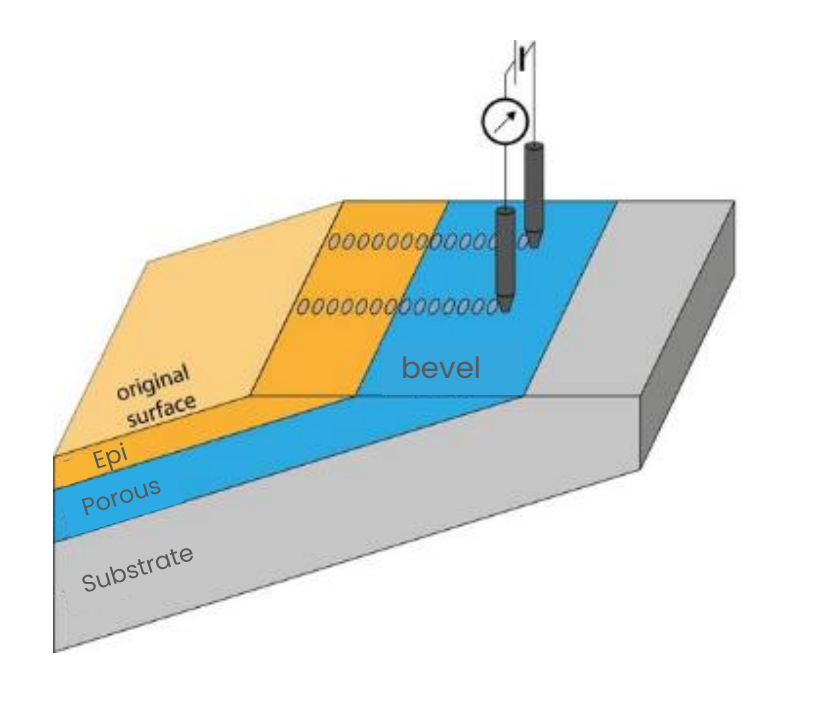
J. Electrochem. Soc., Vol. 138, No. 11, November 1991

Back in 1991, Anderson described a 'depletion region' surrounding the pores. As these depletion regions merged, the porous silicon became 'fully depleted' of charge carriers.

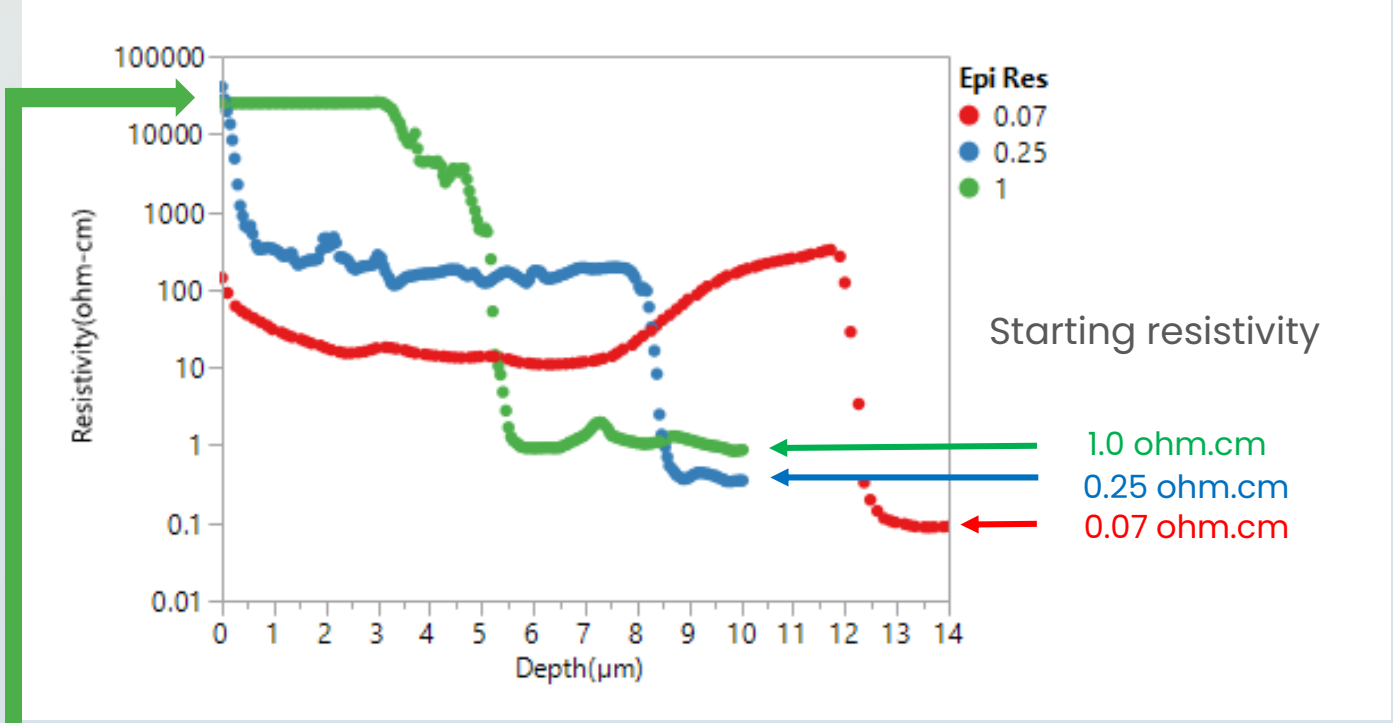
Quote:

"For porous silicon formed from a 30-50 Ωcm boron doped (p-type) substrate, the variations of zero-bias capacitance and conductance indicate (for layers from 0.34 to 4.6 μm thick) that the porous layer is fully depleted of free carriers, and the resistivity is 1.6 x 10^7 Ωcm".

Spreading resistance profiling



Basically a 4pt probe stepped across a ground bevel edge to exaggerate the layer thicknesses.

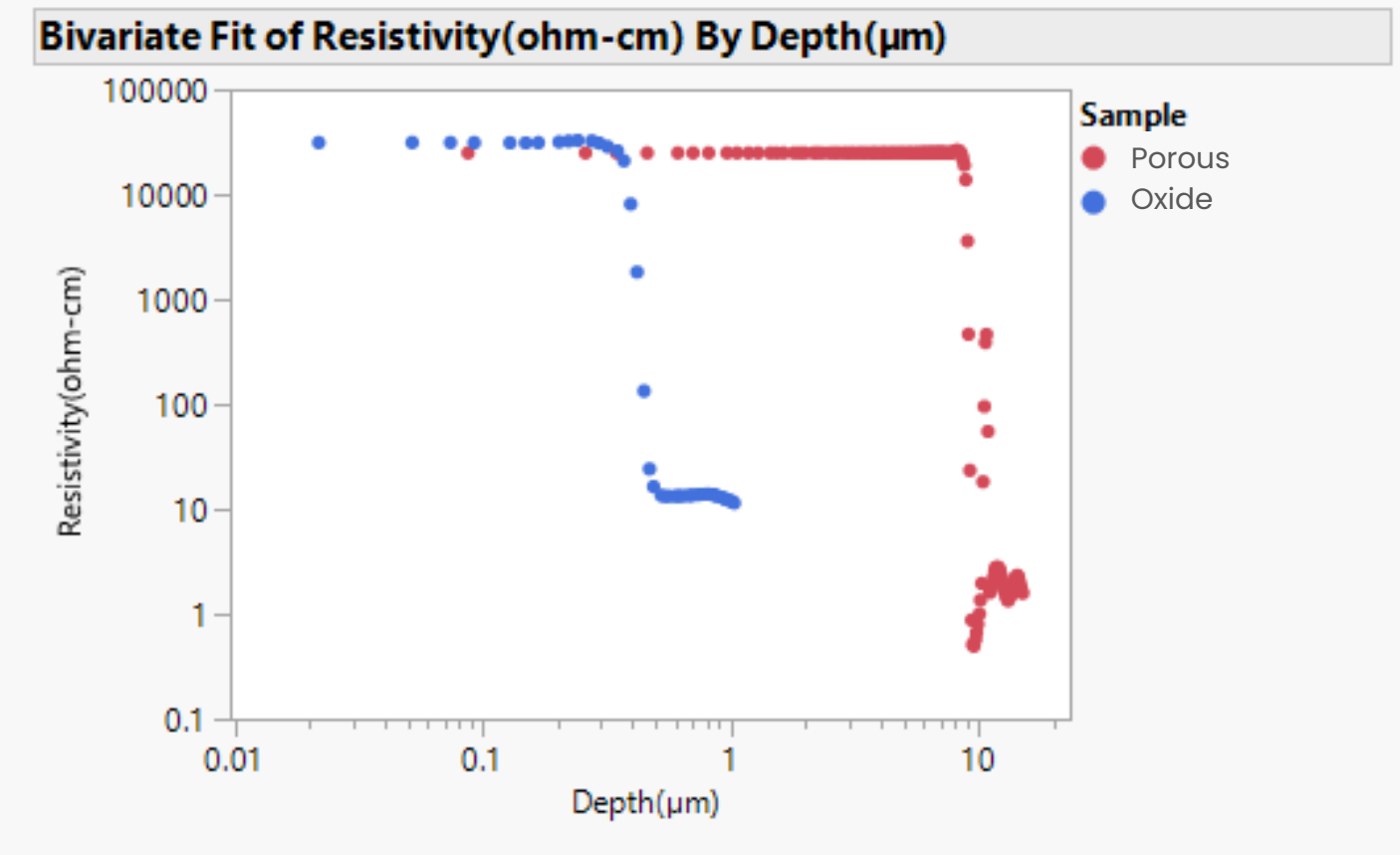


Carrier depletion regions widen as initial doping level decreases.

At ~1ohm.cm depletion regions merge and porous region becomes 'fully depleted'.

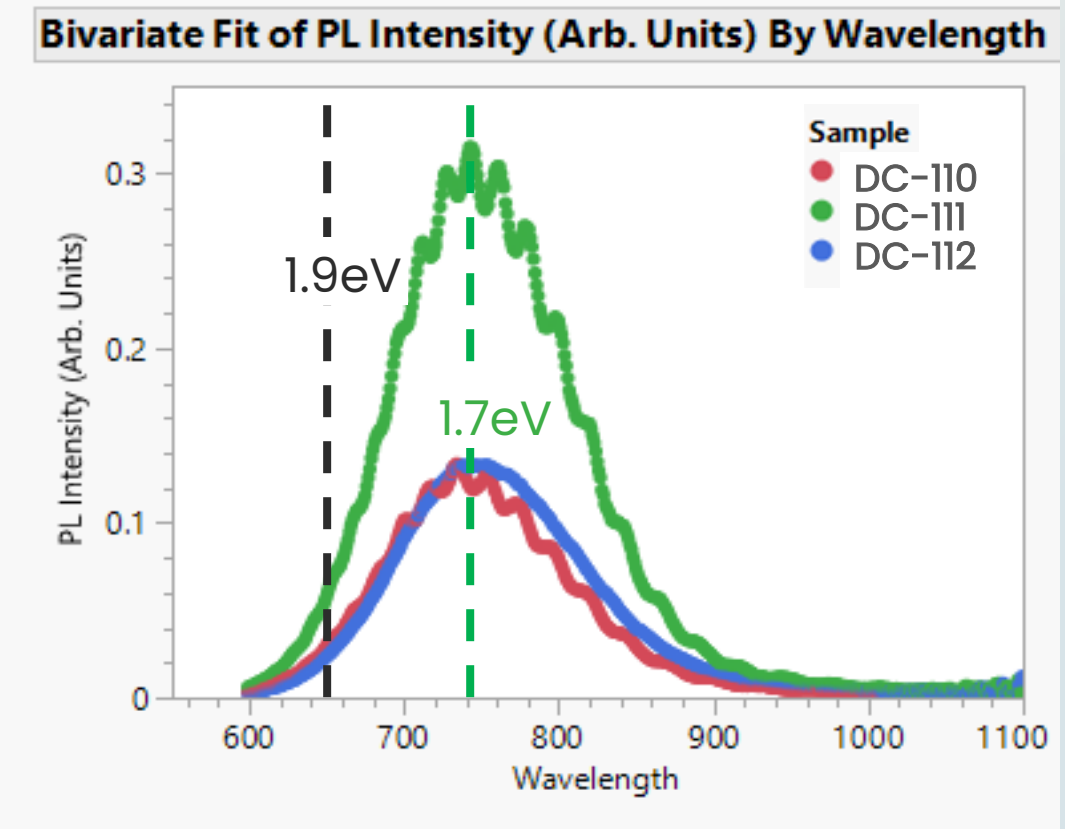
Porous vs. thermal oxide

10um Porous vs. 500nm Thermal Oxide



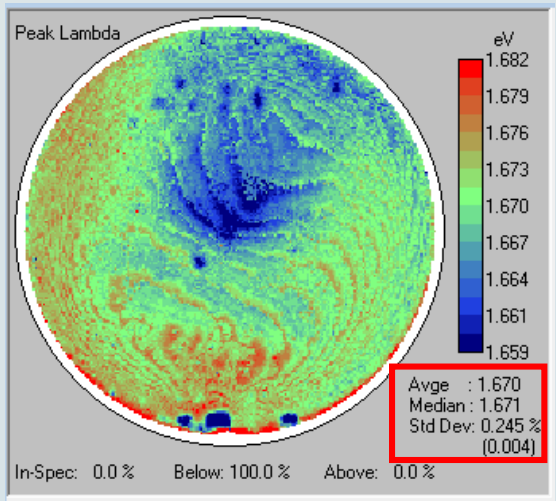
SRP measurement compliance limited at ~30,000ohm.cm

Porous silicon PL



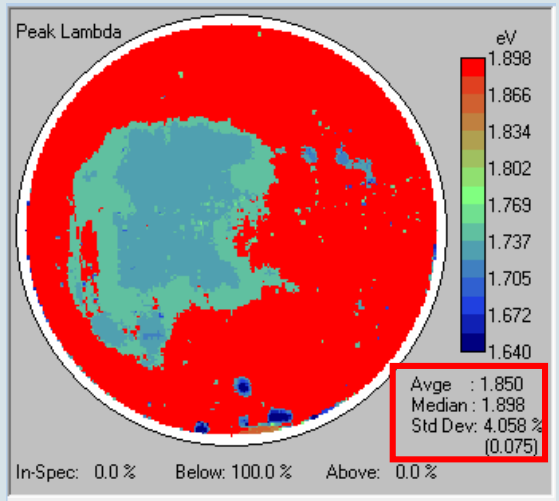
Bulk silicon bandgap = 1.1ev

31,000 point PL map



Porous wafer A

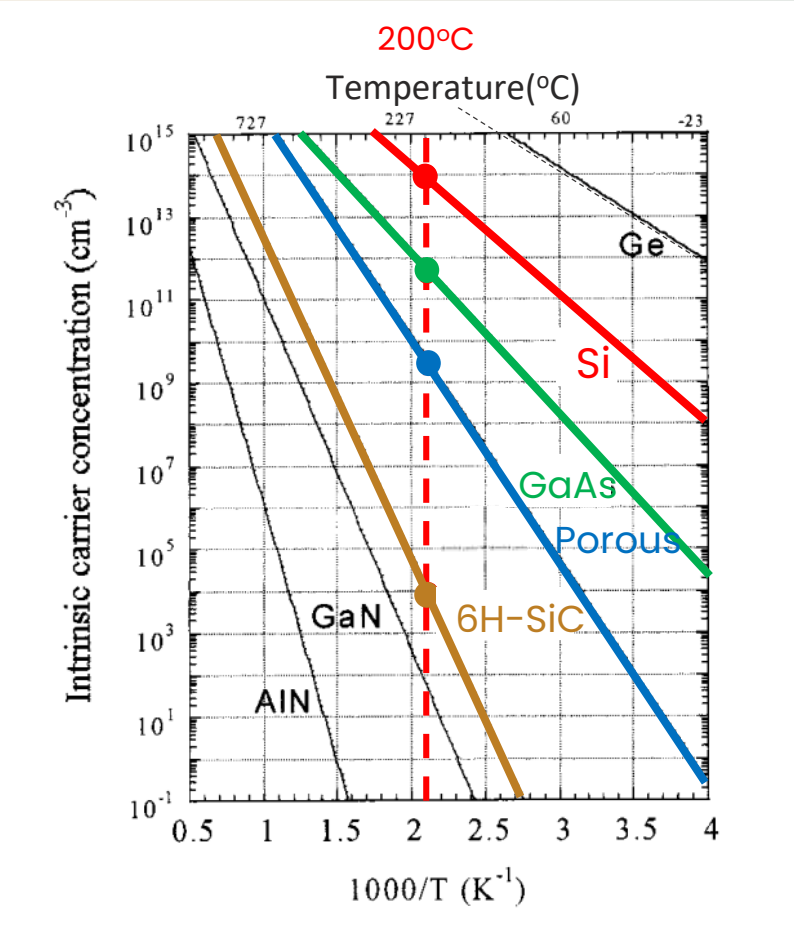
Eg = 1.7eV



Porous wafer B

Eg = 1.9eV

Intrinsic carriers



Porous →

$$N_i = \sqrt{N_c N_v} exp\left[-\frac{E_g}{2k_b T}\right]$$

The intrinsic carrier concentration of a semiconductor is exponentially proportional to the bandgap

Semiconductor	Bandgap (eV)	Intrinsic Carrier Concentration at 200C (cm-3)
Germanium	0.67	1e16
Silicon	1.12	1e14
GaAs	1.42	6e11
Porous	1.7-1.9	~5e9
6H-SiC	3.02	1e4

At 200C, Porous Silicon with Bandgap of 1.9eV would have 4-5 orders of magnitude fewer thermally generated free charge carriers than high resistivity silicon with a bandgap of 1.1eV

RF characterisation of porous silicon

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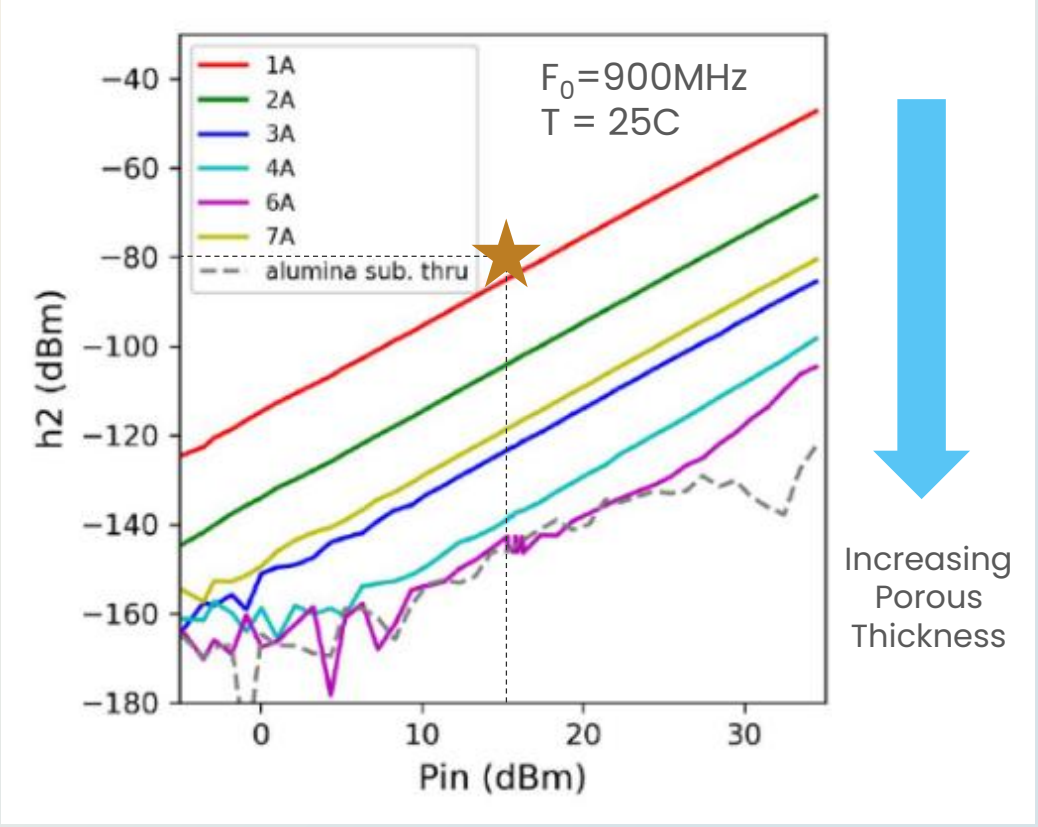
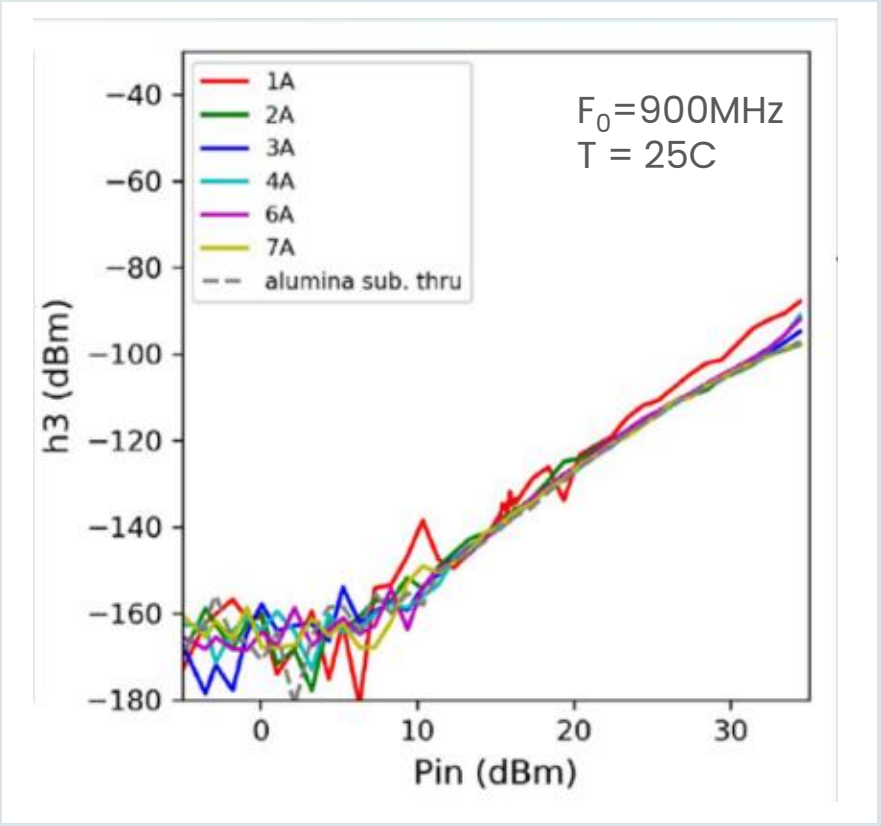
Porous harmonics vs. Thickness

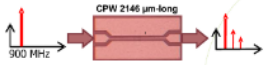
Second Harmonic F_o = 900MHz



Third Harmonic F_o = 900MHz

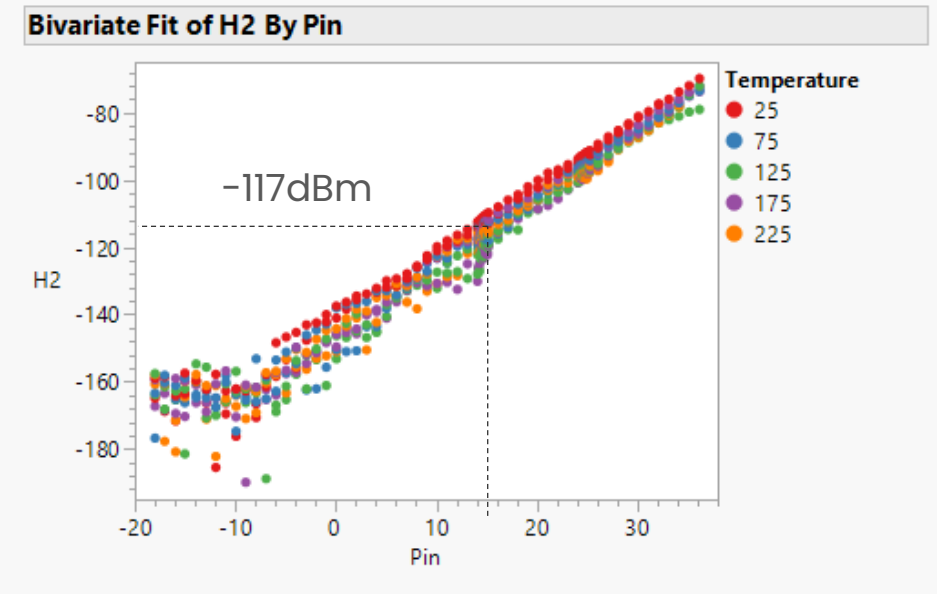


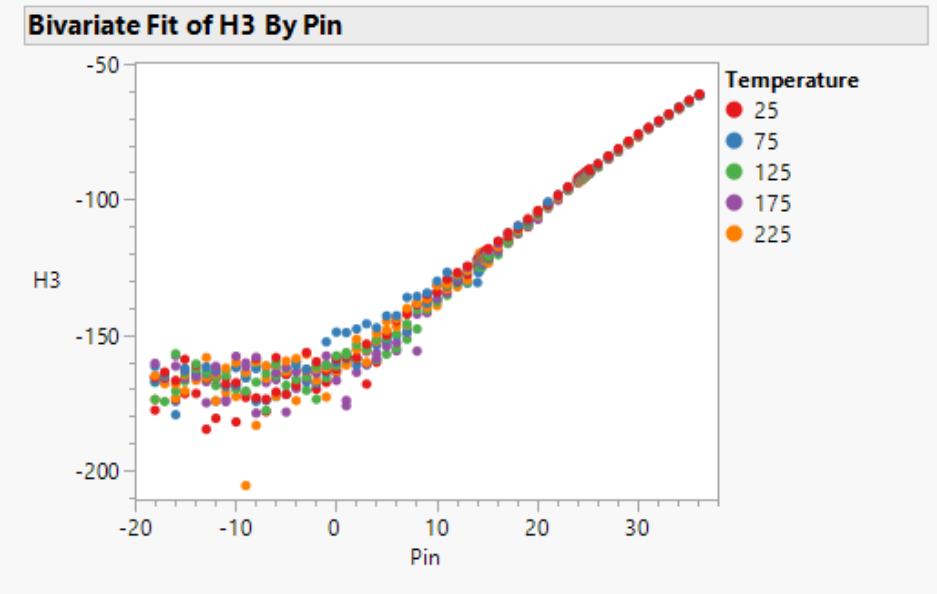
incize

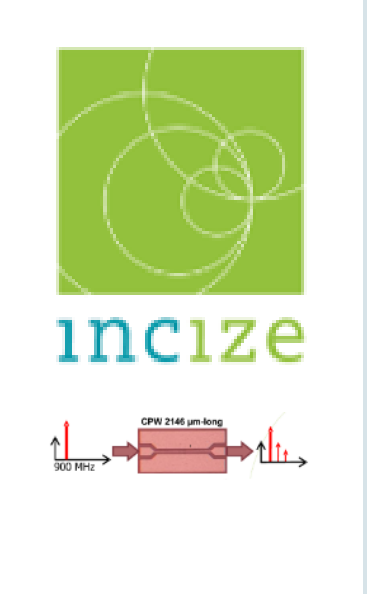


Porous harmonics vs. temp

F_o = 900MHz



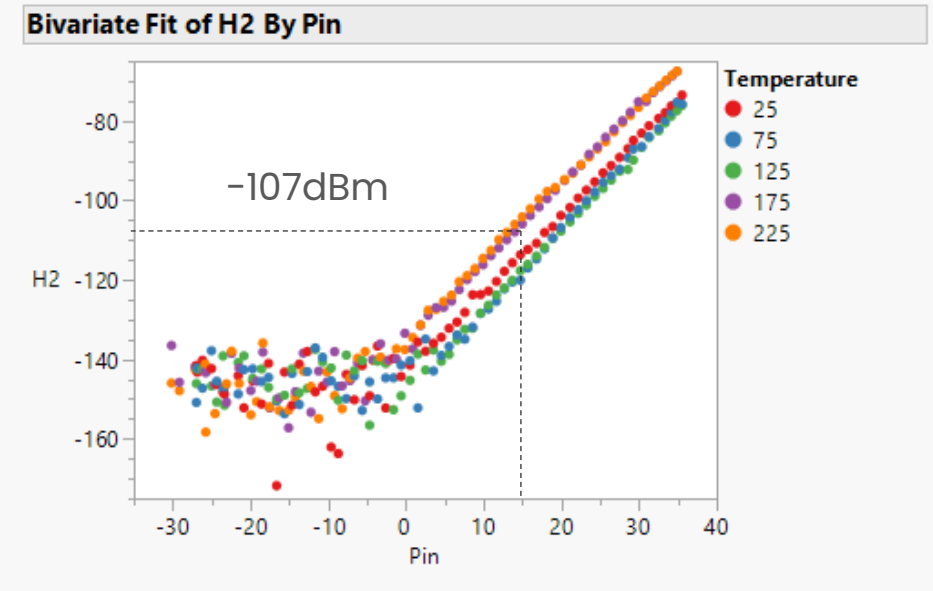


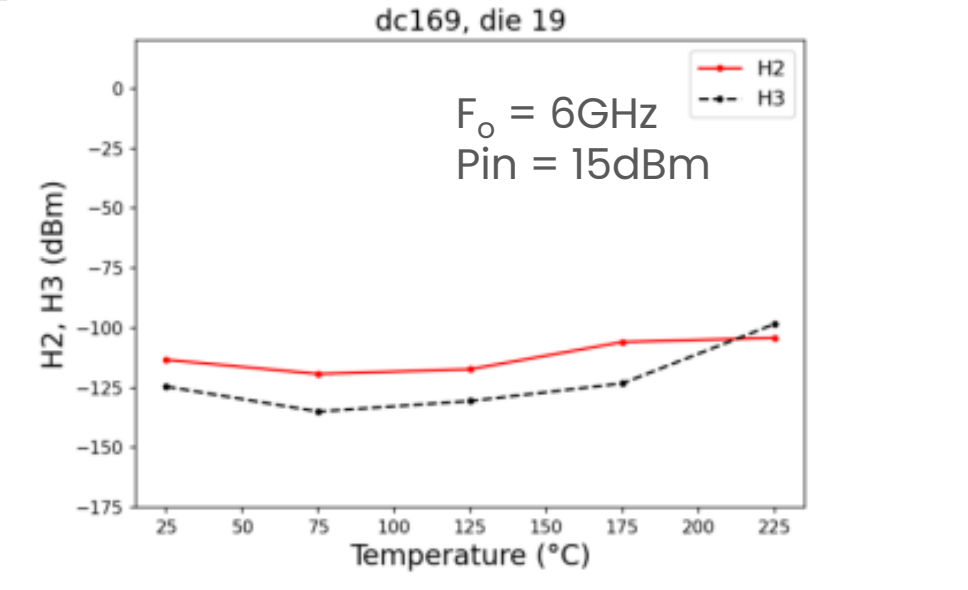


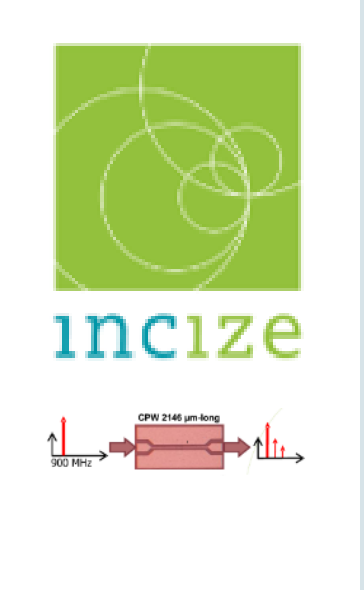
[F_o=900Mhz] H2 and H3 linear and stable to Pin = 36dBm and up to 225C

Porous harmonics @ 6GHz

F_o = 6GHz

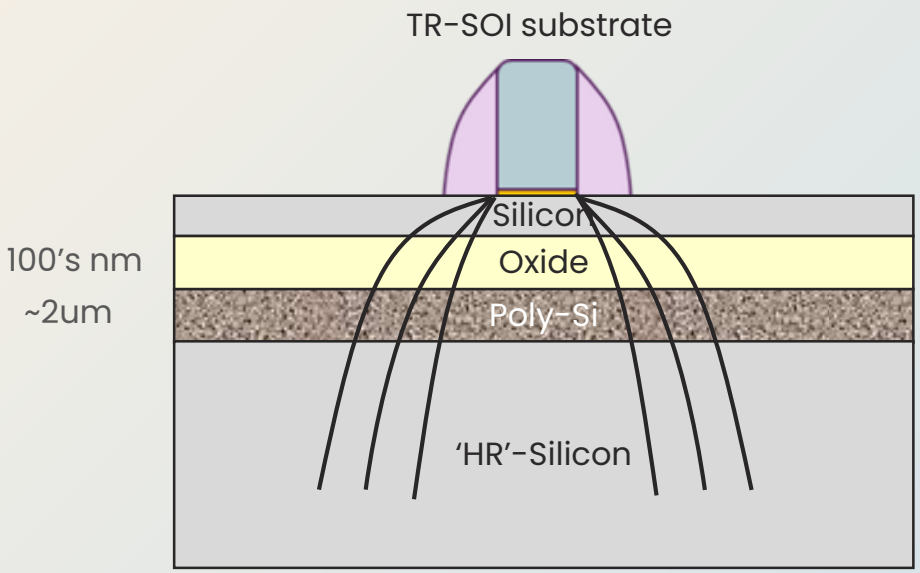




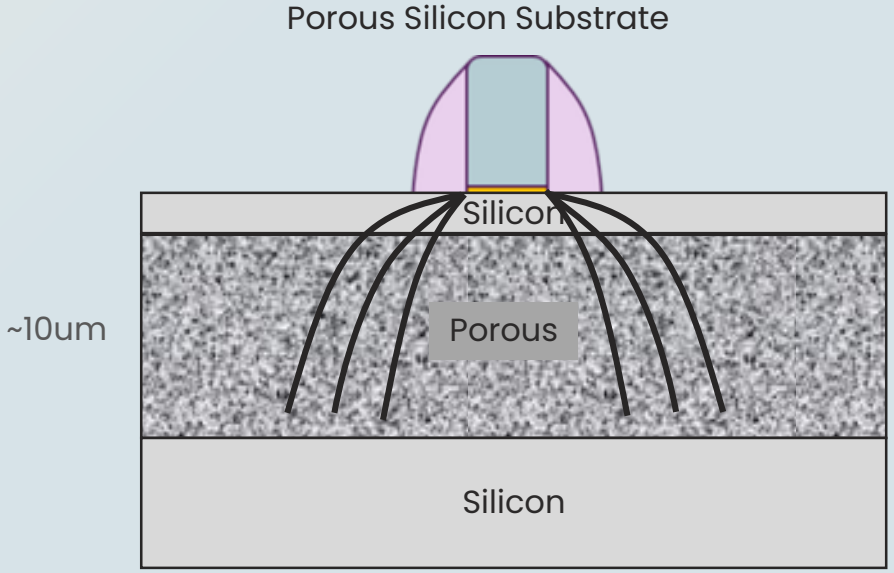


[F_o=6GHz] H2 and H3 linear and stable to Pin = 36dBm and up to 225C

Intrinsic carriers



- RF fringing fields penetrate into the 'High Res' silicon substrate.
- Silicon has a low bandgap of 1.1eV.
- At device operating temperatures, significant amount of intrinsic carriers are generated:
  - 1e14cm^{-3} @ 200C
  - 150ohm.cm
- High Res substrate is not so high res at device temps !



- RF fringing fields confined within thick porous silicon layer.
- Porous Silicon has an increased bandgap of 1.9eV.
- At device operating temperatures, minimal thermal carriers are generated
  - 5e9cm^{-3} @ 200C
  - >100,000 ohm.cm

Literature

Rack et al, UCL

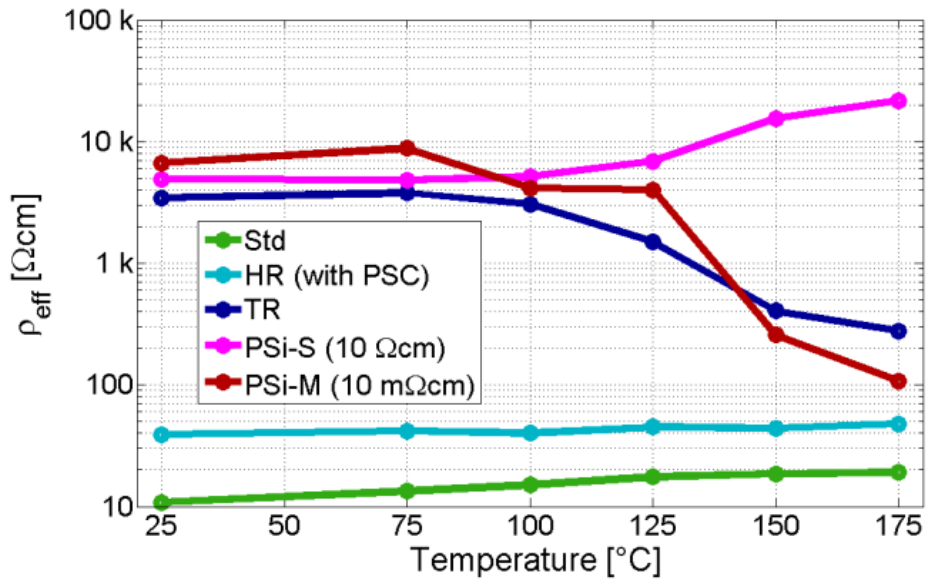


Fig. 6. Effective resistivity averaged between the beginning of the quasi-TEM mode (different for each substrate) and 10 GHz and extracted at different temperature points ranging from 25 °C to 175 °C for the five Si-based substrates.

Rack et al have compared the effective resistivity of various substrates as a function of temperature.

The porous (FD) silicon maintains its Effective Resistivity up to 175C.

Note the large degradation in effective resistivity of **Trap Rich** and **Porous (non-FD)** substrates as a function of temperature.

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 65, NO. 5, MAY 2018 1887

Small- and Large-Signal Performance Up To 175 °C of Low-Cost Porous Silicon Substrate for RF Applications

Martin Rack, Yasmina Belaroussi, Khaled Ben Ali, Gilles Scheen, Babak Kazemi Esfeh, and Jean-Pierre Raskin

Epitaxy on porous silicon

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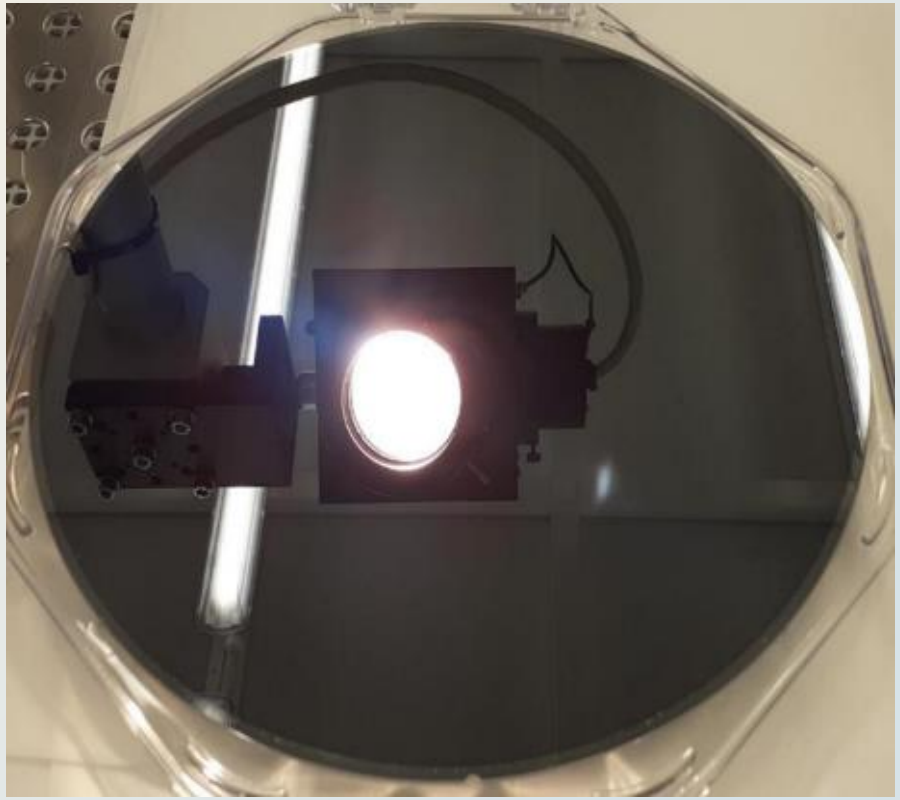
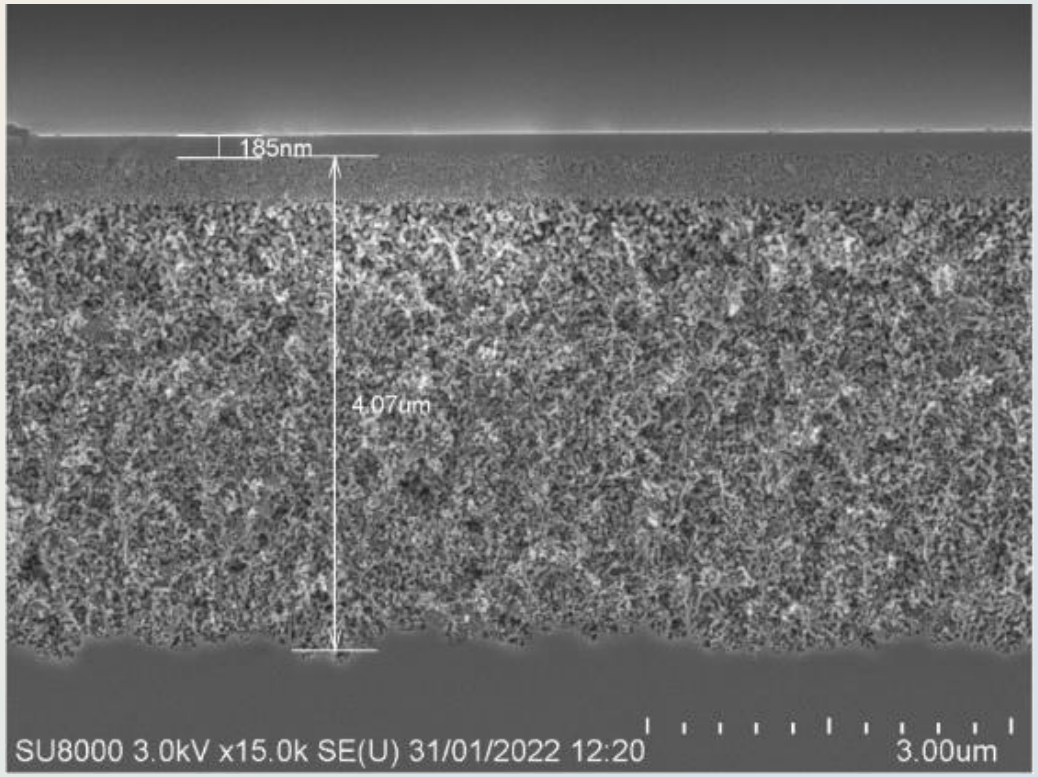
200mm epi on porous

As etched



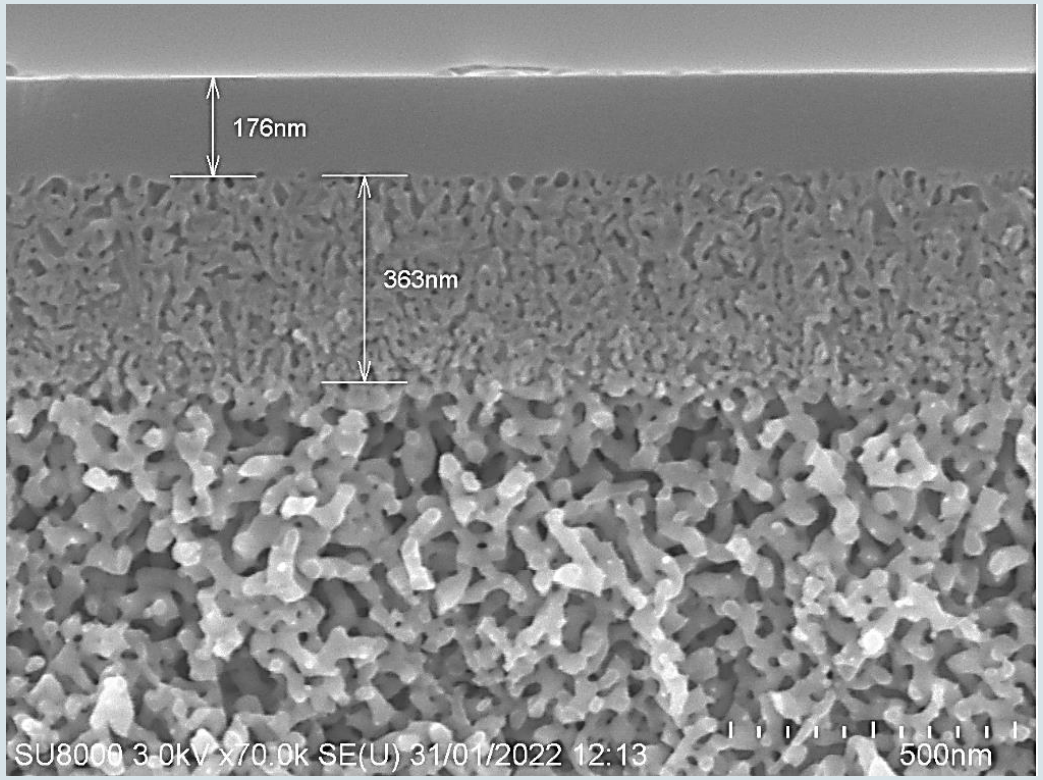
Post 180nm epi

Epitaxy on porous silicon (SEM)



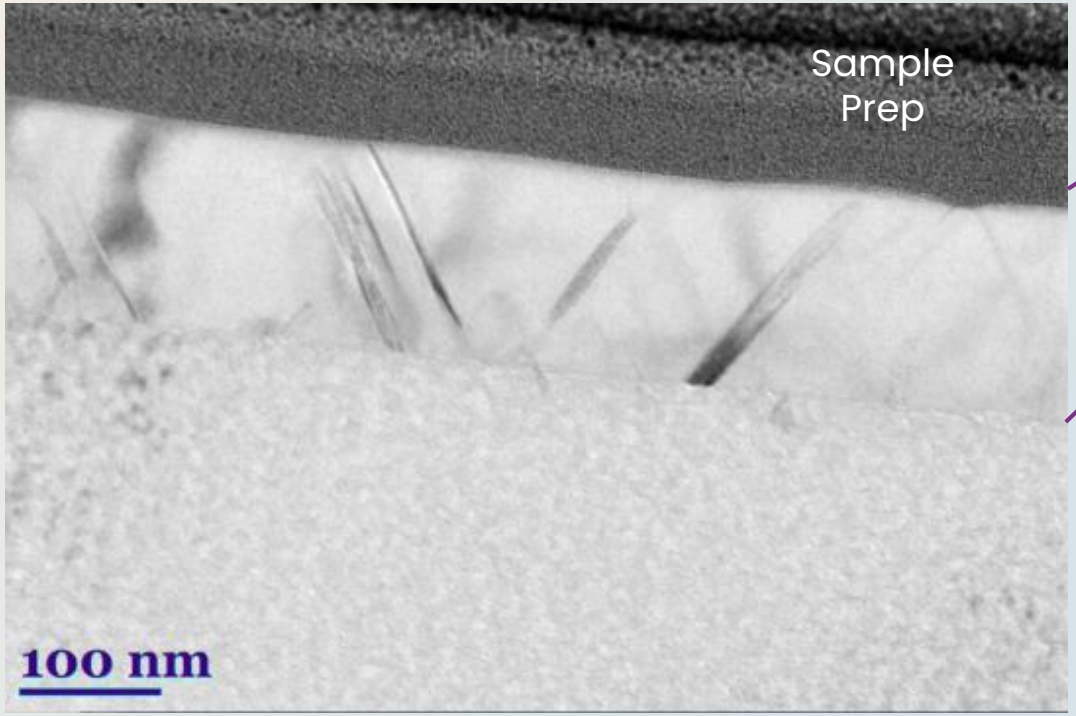
Epi Device Channel

Porous Region



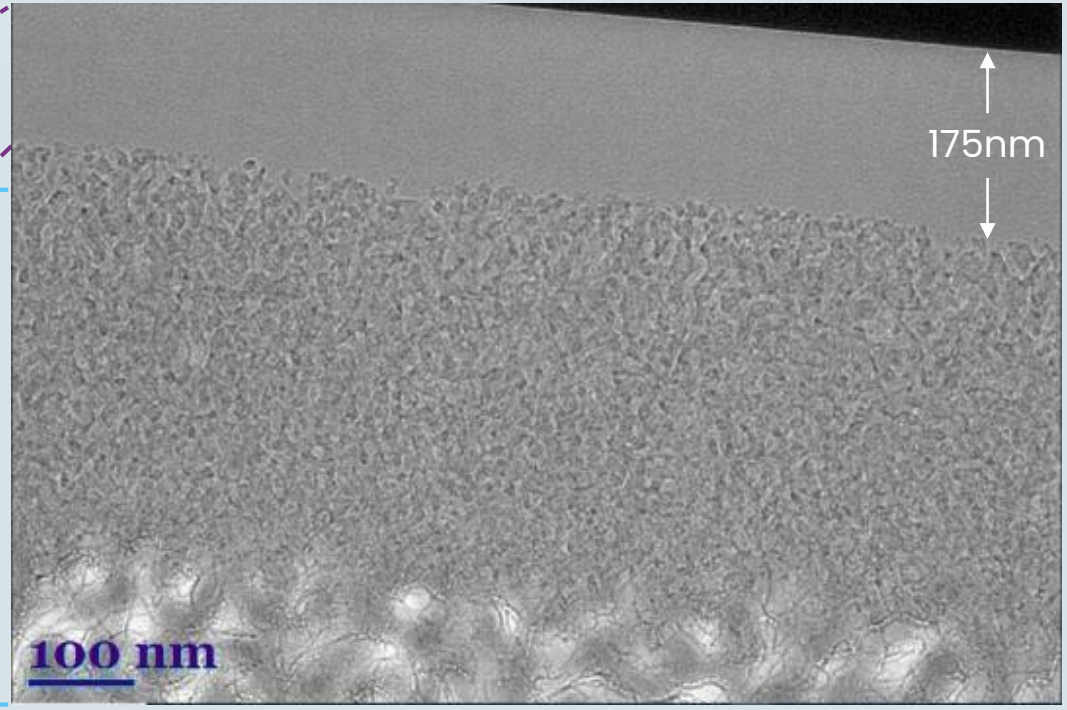
Epitaxial defects (TEM)

Non optimised process



High defectivity epi

Optimised process

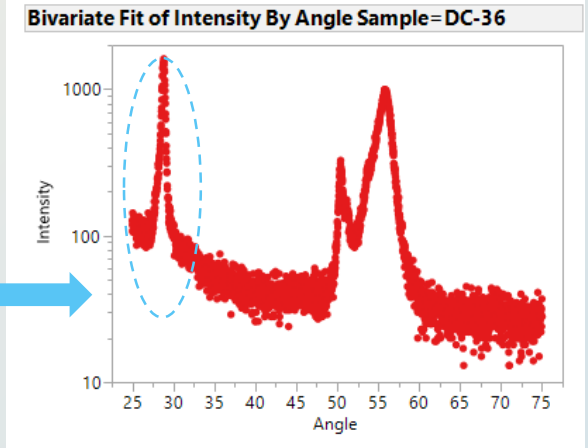


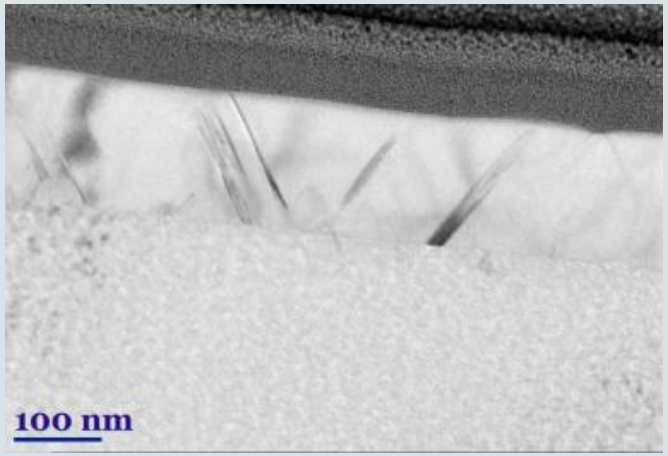
Defect free epi

Grazing angle X-ray diffraction

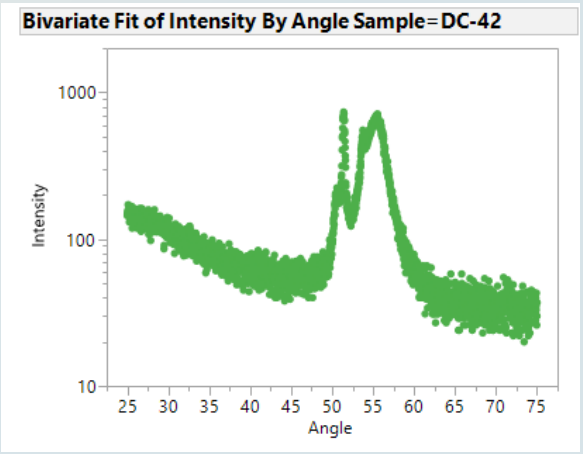
High defectivity epi

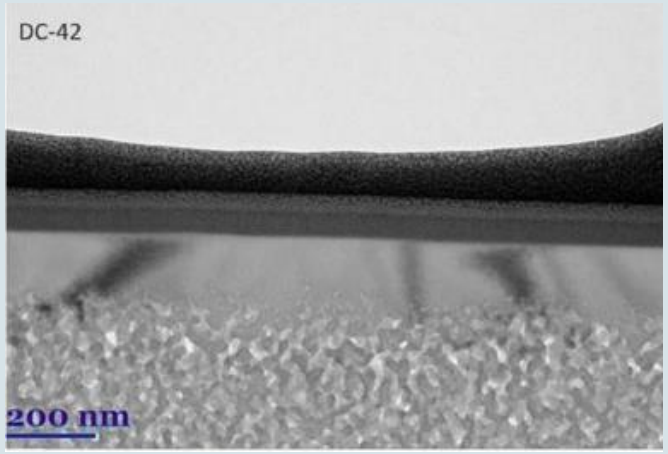
XRD Peak apparent in defective silicon due to different crystallographic orientations



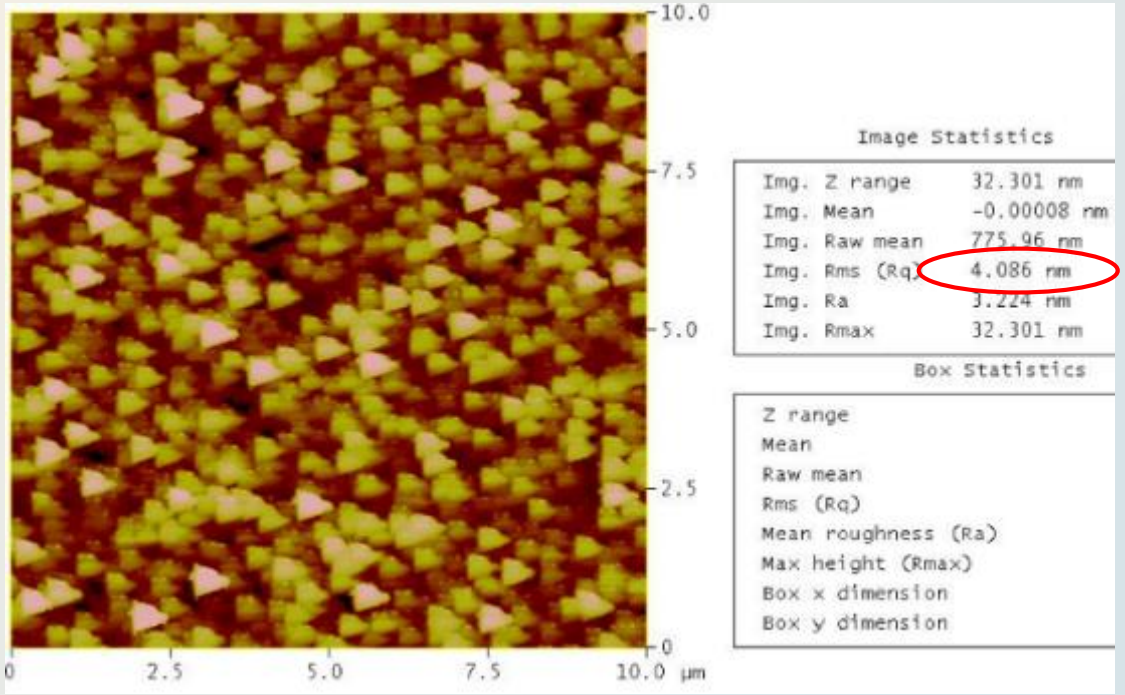


Defect free epi

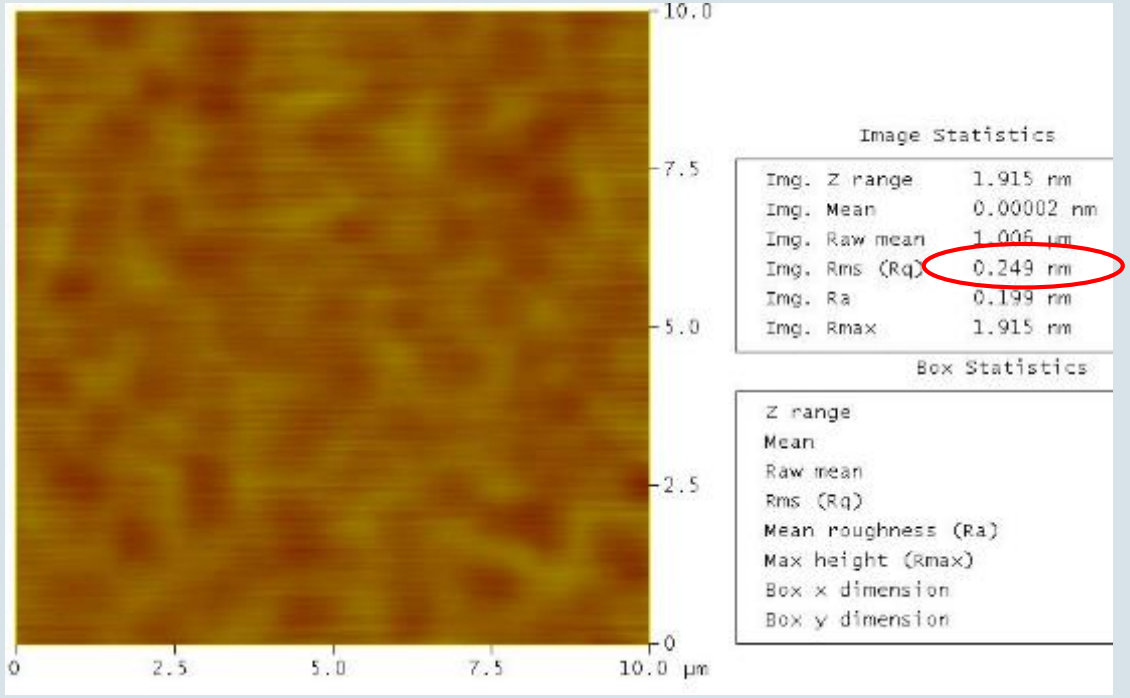




Epi surface roughness (AFM)



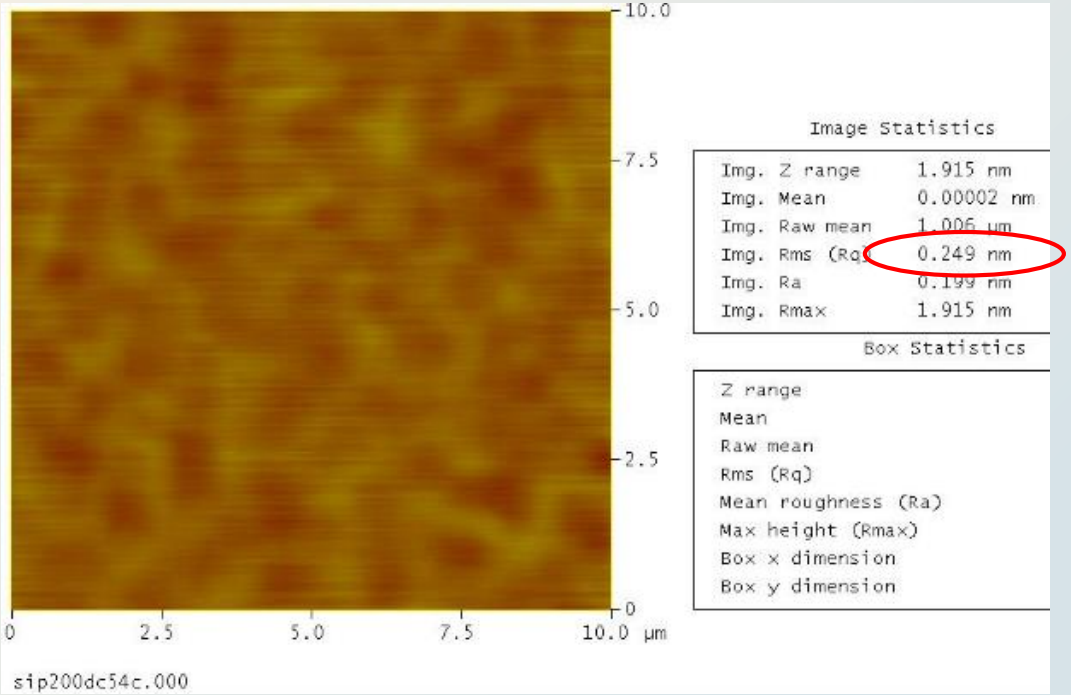
High defectivity epi



Defect free epi

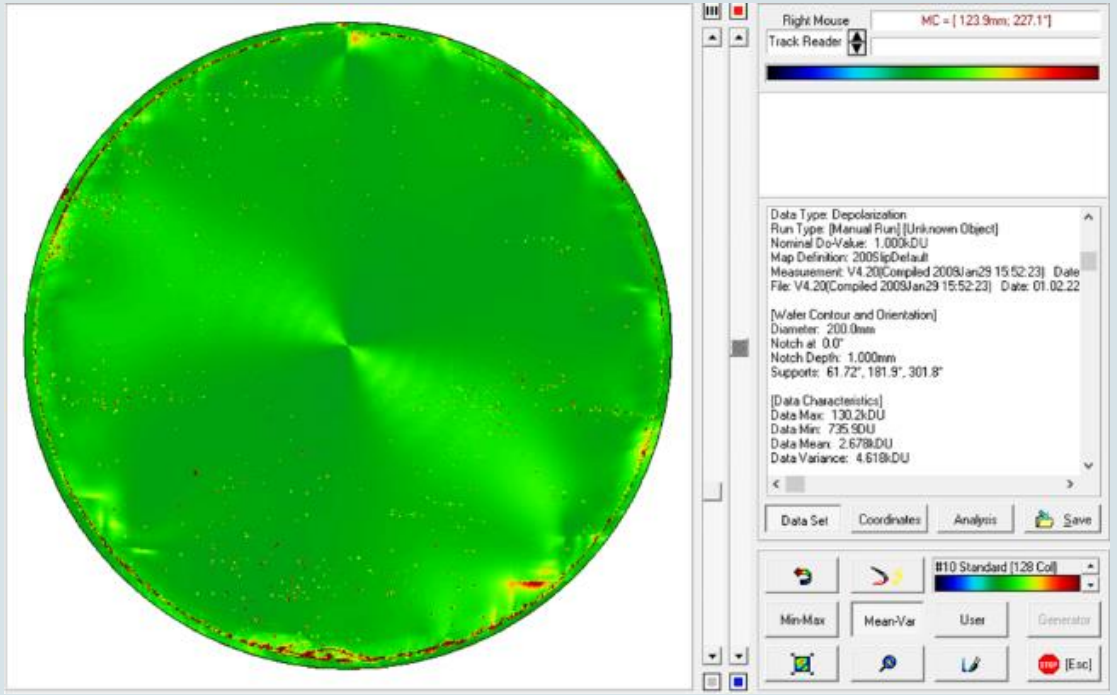
- Epi Surface Roughness = 0.25nm
- Comparable to Prime Silicon wafer

Epi on thin porous



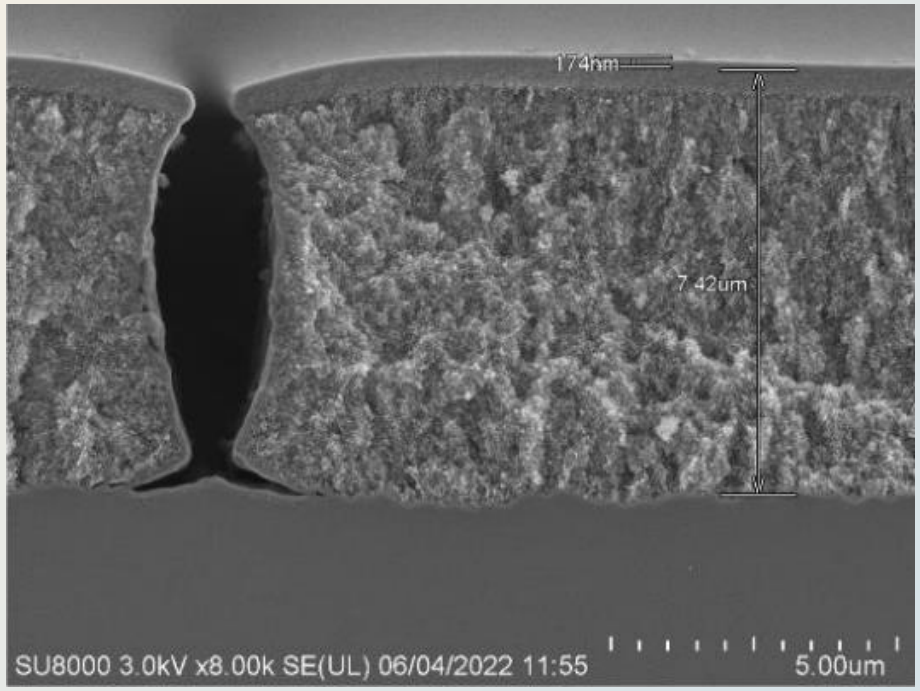
Sub-nm surface roughness

Scanning transmission IR image (TePla)

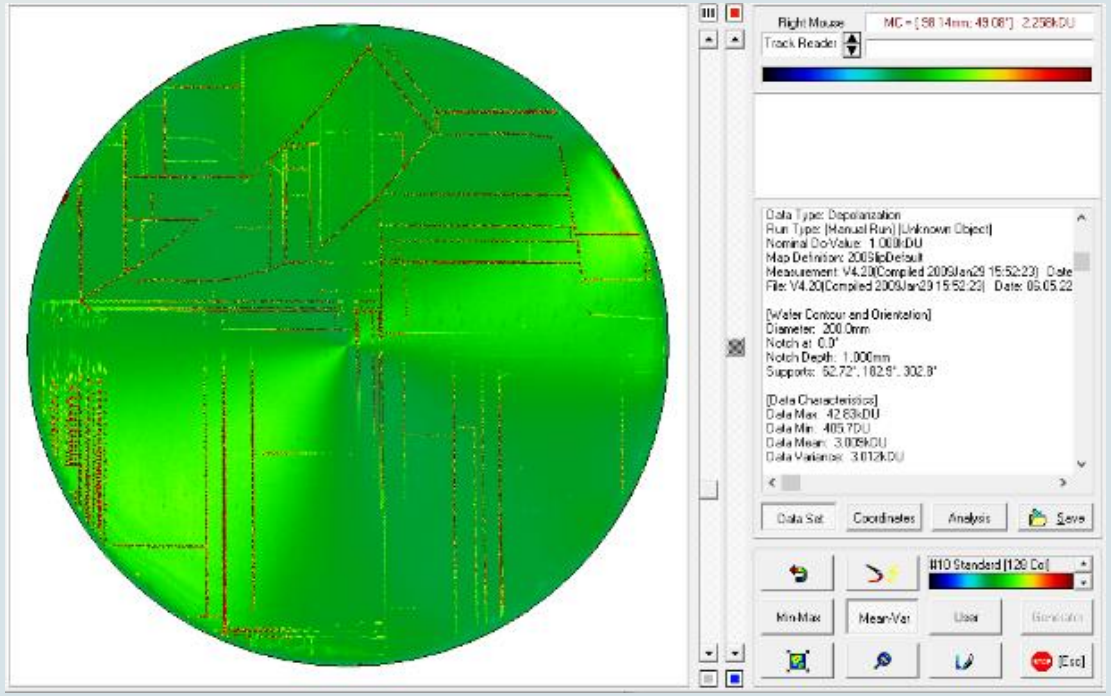


No cracking observed at <5um porous thickness

Epi on thick porous

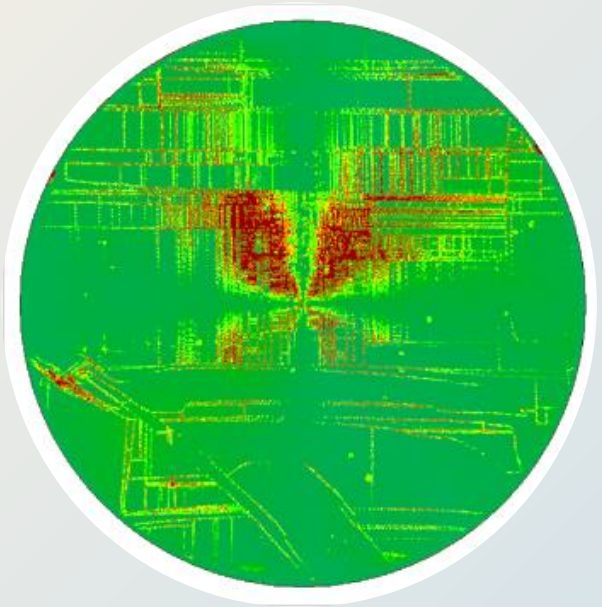


Cracking observed at Porous Thickness ~8um



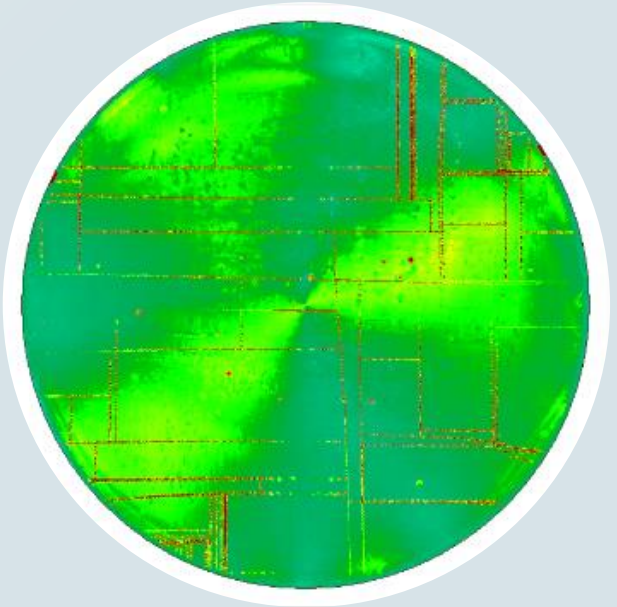
Scanning Transmission IR Image (TePla)

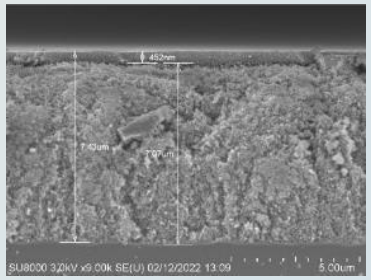
Etch optimisation



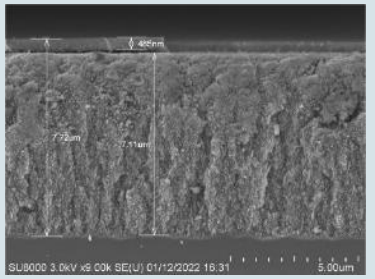
Post Epi IR Imaging

Improved Porous Etch Conditions





7.1um Porous

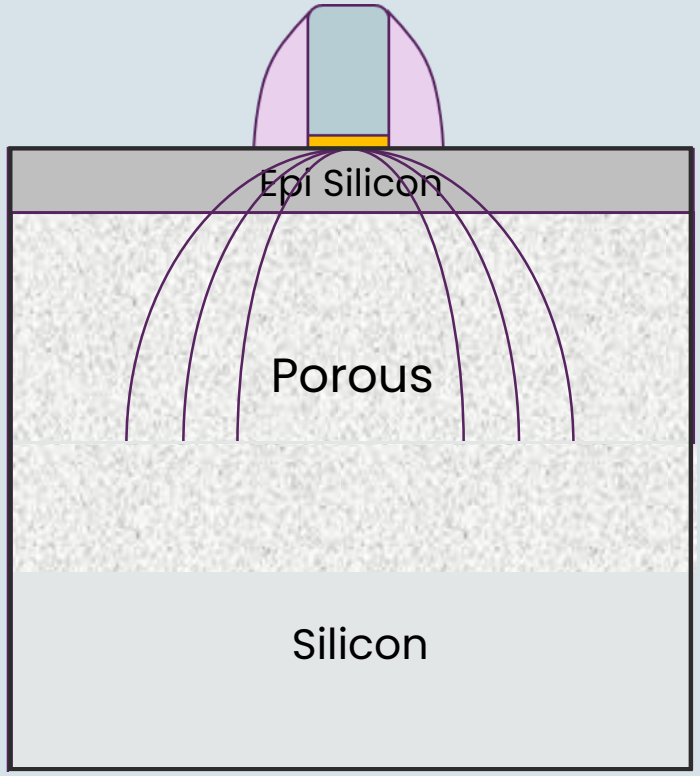


7.1um Porous

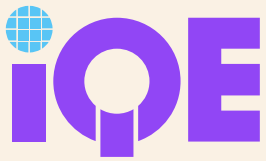
Conclusion

Porous silicon excellent candidate for RF applications:

- **Carrier depletion leads to ultra-high resistivity.**
  - Excellent Harmonic Performance.
- **Increased Porous Bandgap leads to significant reduction in thermally generated free carriers:**
  - Linear RF Performance up to 225C.
- **Porous silicon acts like an amorphous dielectric, but maintains its crystallographic nature:**
  - Ability to grow single crystal, defect-free, device channels.
  - Channel thickness uniformity dictated by epi.



Thank you



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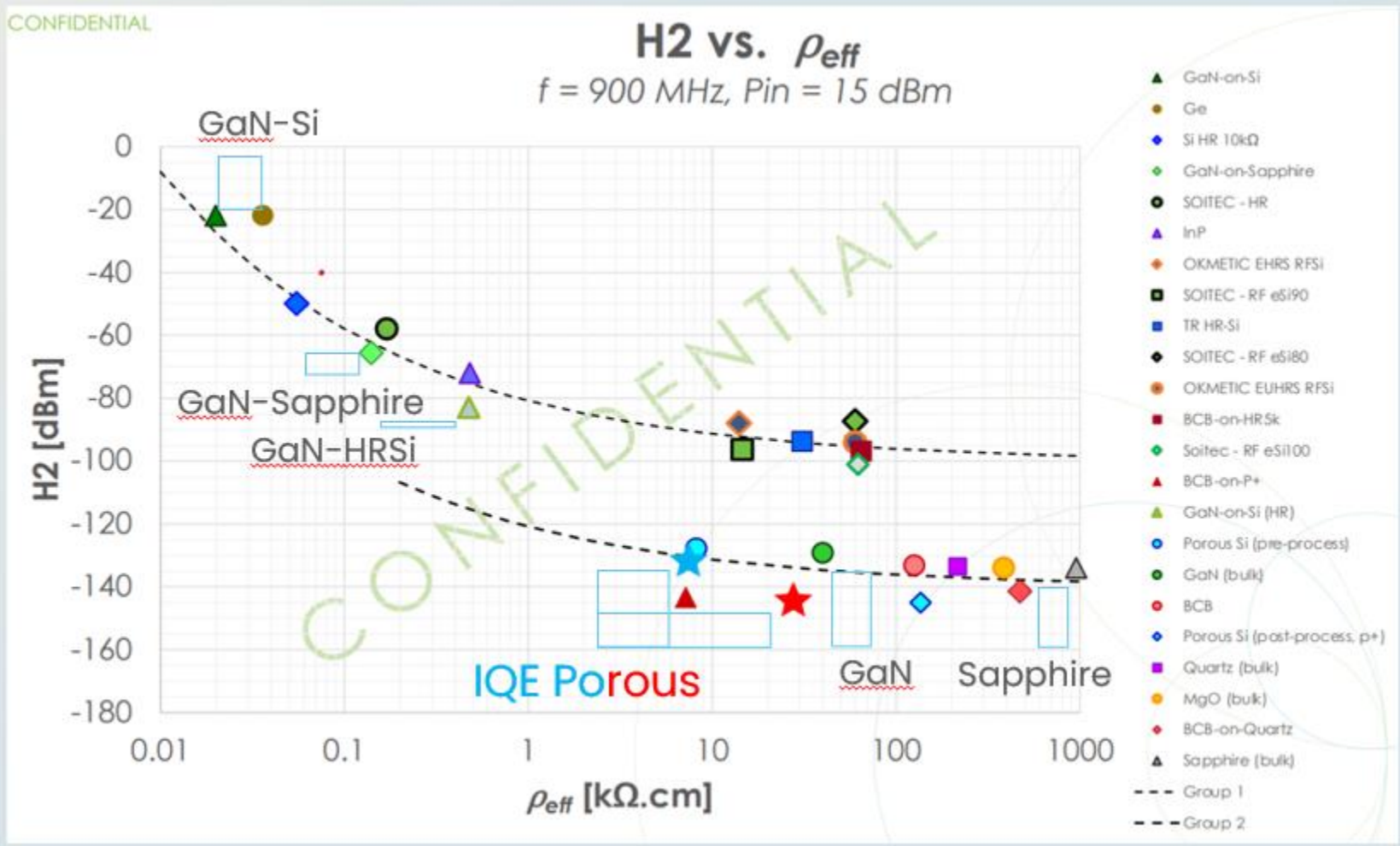
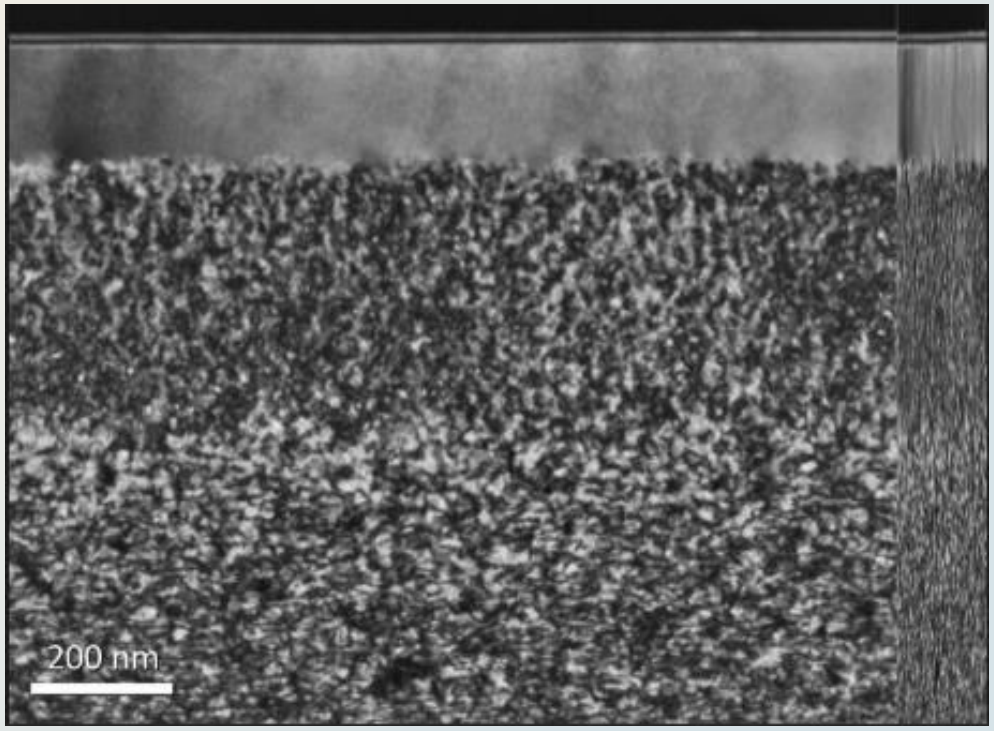
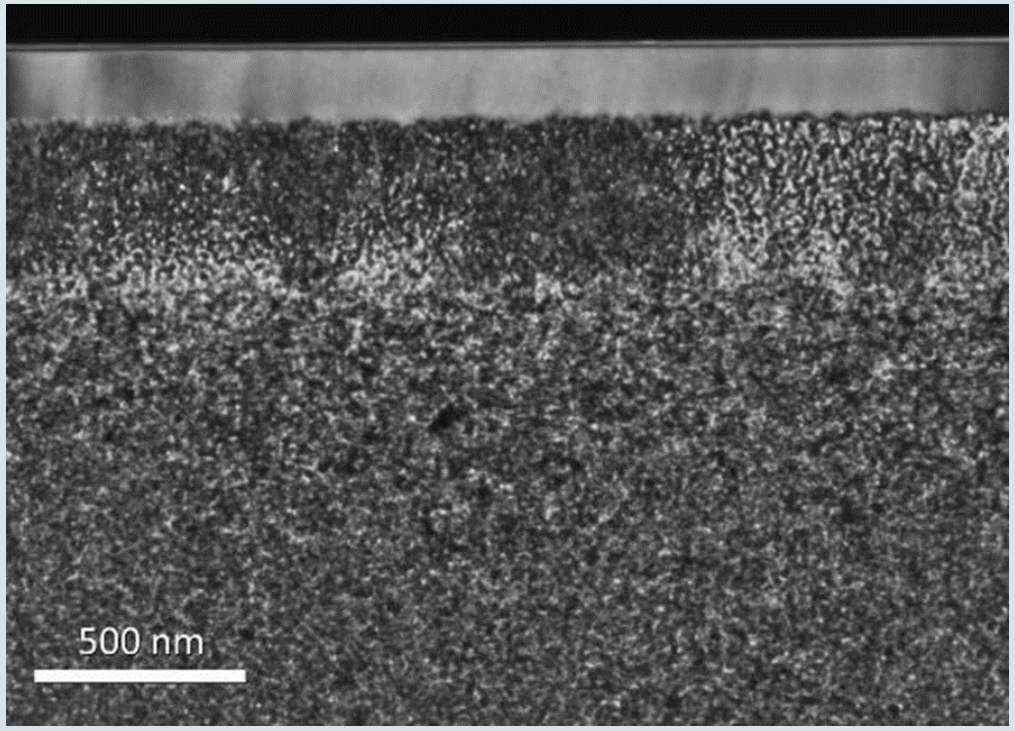


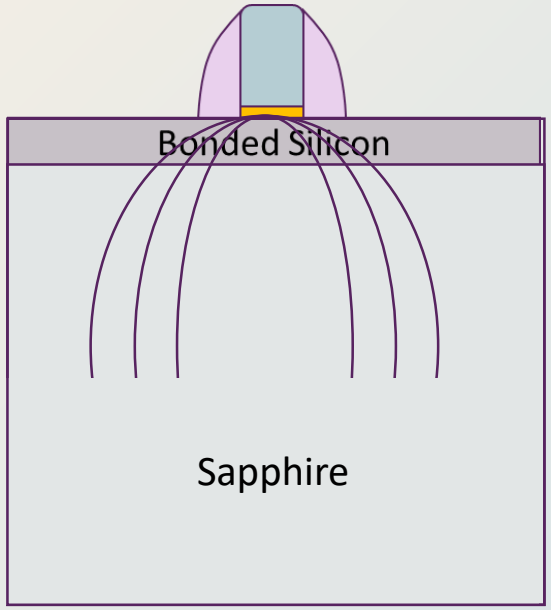
Epi on porous

XTEM



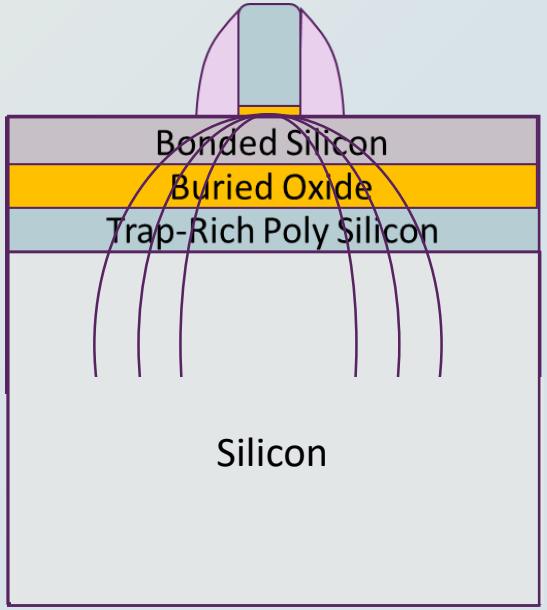


BSOS



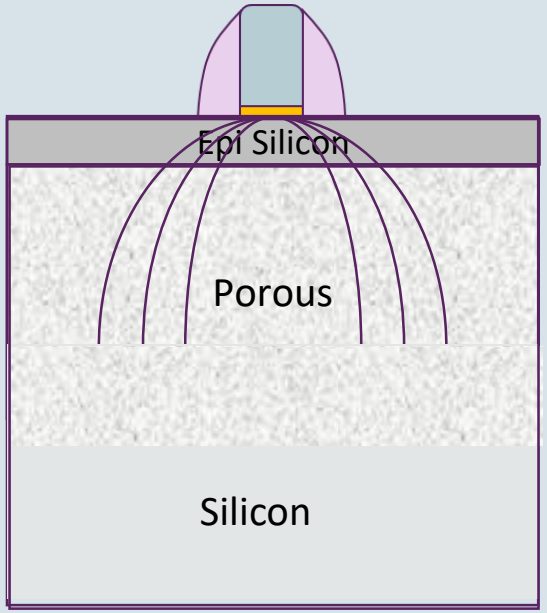
✔ RF Fields contained within fully insulating sapphire.

TR-SOI



✘ RF Fields penetrate the High resistivity silicon.

Porous



✔ RF Fields contained within Ultra High Resistivity Porous.